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(54) Method of manufacturing semiconductor wafer method of using and utilizing the same

(57) A process for manufacturing a semiconductor wafer which has superior suitability for mass production and reproducibility. The process comprises the steps of preparing a first member which has a monocrystalline semiconductor layer on a semiconductor substrate with a separation layer arranged therebetween with a semiconductor wafer as the raw material, transferring the monocrystalline semiconductor layer onto a second member which comprises a semiconductor wafer after separating the monocrystalline semiconductor layer through the separation layer, and smoothing the surface of the semiconductor substrate after the transferring step so as to be used as a semiconductor wafer for purposes other than forming the first and second members.

FIG. 4A

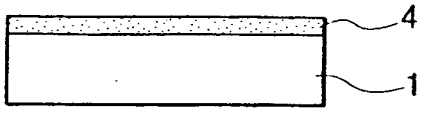

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FIG. 4B

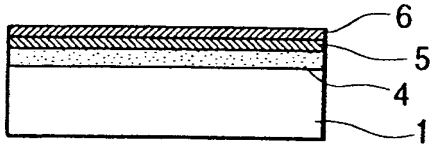


FIG. 4C

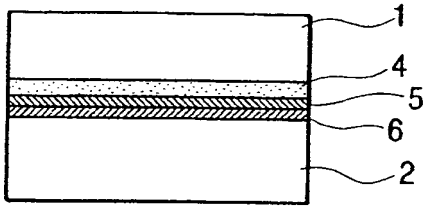


FIG. 4D

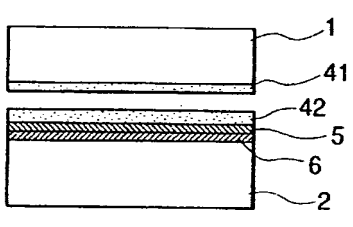


FIG. 4E

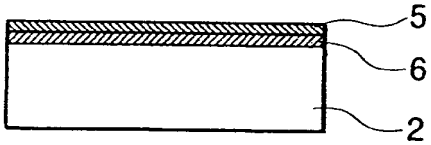
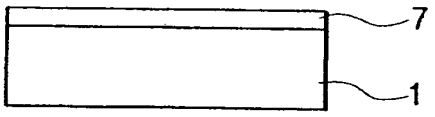


FIG. 4F

FIG. 4G



Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention relates to a process for manufacturing a semiconductor wafer and also to a process for using and utilizing such a semiconductor wafer.

[0002] More particularly, the present invention relates to a process for manufacturing a semiconductor wafer that can be used for producing a semiconductor device such as a microprocessor, a memory, a logic circuit, a system LSI, a solar battery, an image sensor, a light emitting device or a display device, as a monitor wafer such as a film thickness monitor to be used for forming a film, an etching depth monitor to be used for an etching operation or a particle monitor to be used for detecting and counting foreign particles or as a dummy wafer to be used in a processing system in order to regulate various processing conditions for film formation, heat treatment, doping or etching. It also relates to a method of using and utilizing such a semiconductor wafer. Specifically, the present invention is adapted to manufacture semiconductor wafers of different types that can be used and utilized in different applications.

Related Background Art

[0003] Semiconductor wafers having layers of various semiconductor materials such as Si, GaAs, InP and GaN are known. Particularly, SOI wafers comprising a support substrate having an insulating surface and a semiconductor layer formed thereon are attracting attention as they are highly adapted to preparing semiconductor devices that operate at high speed with a low power consumption. For the purpose of this invention, an SOI wafer refers to a wafer carrying a semiconductor on an insulator, which may not necessarily be a wafer carrying silicon on an insulator.

[0004] Known SOI wafers include SIMOX wafers prepared through oxygen ion implantation and heat treatment and bonded wafers such as those described in Japanese Patent Application Laid-Open No. 5-211128, U.S. Patent No. 5,374,564 and Japanese Patent Application Laid-Open No. 10-200080 and prepared through hydrogen ion implantation and peeling as well as the one described in International Patent Publication W098/52216 and prepared through plasma immersion ion implantation (PIII). Japanese Patent Application Laid-Open No. 2608351 and U.S. Patent No. 5,371,037 describe respective methods of preparing a high quality SOI wafer by transferring an epitaxial layer on a separate support substrate.

[0005] Japanese Patent Application Laid-Open No. 7-302889 (U.S. Patent No. 5,856,229) proposes an improved method for transferring an epitaxial layer.

[0006] FIGS. 17A through 17E schematically illustrate the known method for transferring an epitaxial layer.

[0007] Firstly, as shown in FIG. 17A, a semiconductor wafer that is an Si wafer (which may be referred to as prime wafer, bond wafer, device wafer or seed wafer) is brought in and the surface anodized to produce a porous layer 4 on the surface.

[0008] Then, as shown in FIG. 17B, a non-porous monocrystalline semiconductor layer 5 is formed on the porous layer 4 by epitaxial growth, typically using a CVD technique.

[0009] Thereafter, as shown in FIG. 17C, the surface of the epitaxial layer (non-porous monocrystalline semiconductor layer) is oxidized to produce an insulating layer 6. Then, said insulating layer 6 is brought to contact with and bonded to the surface of another semiconductor wafer 2 (or a piece of quartz glass). Thus, a multilayer structure containing the epitaxial layer 5 in the inside is prepared.

[0010] Then, as shown in FIG. 17D, the multilayer structure is subjected to external force or internal stress typically by inserting a wedge into a lateral side thereof or heating the multilayer structure in order to split it along the porous layer (reference numerals 41 and 42 in FIG. 17D shows the split porous layer).

[0011] Then, the porous layer 4B remaining on the surface of the epitaxial layer 5 that has been transferred to the second semiconductor wafer 2 (also referred to as handle wafer or base wafer) is removed by wet etching, using a mixture solution of hydrofluoric acid and hydrogen peroxide. Then, as shown in FIG. 17E, the exposed epitaxial layer is smoothed typically by hydrogen annealing to produce a finished SOI that has remarkable characteristics.

[0012] On the other hand, the separated Si wafer still maintains the profile of a thin disk. Therefore, it can be used as Si wafer 1 for preparing another SOI wafer as shown in FIG. 17A for another time after removing the porous layer remaining on the cleaved side thereof also by wet etching, using the same solution. Alternatively, it may be used as semiconductor wafer 2 for preparing another SOI wafer as shown in FIG. 17B.

[0013] As described above, Japanese Patent Application Laid-Open No. 7-302889 discloses a method of reusing a peeled Si wafer as Si wafer 1 as shown in FIG. 17A or as semiconductor wafer 2 as shown in FIG. 17B.

[0014] However, the above described method is accompanied by several problems to be dissolved.

[0015] For instance, when an Si wafer is repeatedly reused as the first wafer, it gradually loses its thickness because

its surface layer is turned into a porous layer for another time and the produced porous layer is subsequently removed. Therefore, each reuse of such an Si wafer may require a cumbersome process of adjusting the conditions under which it is reused by forming a porous layer on the surface to consequently reduce its thickness further. Additionally, if a multilayer structure is produced, it can be sensitively affected by the thickness of the first wafer and those of other layers to become swerved under certain conditions. Thus, it is highly important to rigorously control the thickness of the first wafer.

[0016] Additionally, the damage to the Si wafer that occurred in the separating step may adversely affect the subsequent steps including that of producing a porous layer to make it no longer usable for manufacturing SOI wafers having the same and identical characteristics.

[0017] Still additionally, the process of manufacturing SOI wafers is far more complex than that of manufacturing bulk wafers and hence the yield of manufacturing SOI wafers is normally rather low. In other words, if the reusable first wafer is actually reused as the first or second wafer for preparing another SOI wafer, it may not satisfactorily be used on a commercial basis from the viewpoint of attaining a necessary quality level.

[0018] While the above known method of reusing an Si wafer is intended to reuse the first wafer that is recovered after the process of manufacturing an SOI wafer for manufacturing another SOI wafer of the same quality, the Si wafer is normally short of meeting the requirements of a commercially feasible wafer of the type under consideration.

[0019] Then, such an Si wafer may have no value from the viewpoint of reducing waste and exploiting limited resources in the industry of the near future.

SUMMARY OF THE INVENTION

[0020] An object of the present invention is to provide a process for manufacturing a semiconductor wafer which has superior suitability for mass production and reproducibility.

[0021] It is another object of the present invention to provide a process for manufacturing a semiconductor wafer which improves economic efficiency and provides SOI wafers having excellent quality without decreasing the number of wafers on the market.

[0022] A process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

preparing a first member which has a semiconductor layer on a semiconductor substrate;
transferring said semiconductor layer onto a second member after separating said semiconductor layer from said first member; and
smoothing the surface of said semiconductor substrate after said transferring step so as to use said semiconductor substrate as a semiconductor wafer for purposes other than forming said first and second members.

[0023] Moreover, a process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

preparing a first member which has a semiconductor layer on a semiconductor substrate with a separation layer arranged therebetween;
transferring said semiconductor layer onto a second member after separating said semiconductor layer through said separation layer; and
smoothing the surface of said semiconductor substrate after said transferring step so as to use said semiconductor substrate as a semiconductor wafer for purposes other than forming said first and second members.

[0024] A process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

preparing a first member which has a semiconductor layer on a p-type semiconductor substrate;
separating said semiconductor layer from said first member to transfer the semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate from which said semiconductor layer has been separated, said low concentration p-type semiconductor layer having an impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

[0025] A process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

preparing a first member which has a semiconductor layer on a p-type semiconductor substrate with a separation layer arranged therebetween;

separating said semiconductor layer through said separation layer to transfer the semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate which has been separated through said separation layer, said low concentration p-type semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

[0026] A process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

forming a separation layer within a p-type semiconductor substrate to form a first member which has a semiconductor layer on said separation layer;
separating said semiconductor layer through said separation layer to transfer the semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate which has been separated through said separation layer, said low concentration p-type semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

[0027] A process for manufacturing a semiconductor wafer according to the present invention comprises steps of:

preparing a first member which has a semiconductor layer on a p-type semiconductor substrate with a separation layer arranged therebetween;
bonding said first member with a second member to form a multilayer structure;
conducting heat-treatment of said multilayer structure under an oxidizing atmosphere
separating said multilayer structure through said separation layer to transfer said semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate which has been separated through said separation layer, said low concentration p-type semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

[0028] A process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

preparing a first member which has at least a first semiconductor layer comprising an epitaxial semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of a p-type semiconductor substrate, a separation layer, and a second semiconductor layer, arranged on said p-type semiconductor substrate in that order; and
forming a first semiconductor wafer by transferring said second semiconductor layer onto said second member through the separation step of separating said second semiconductor layer through said separation layer, and forming a second semiconductor wafer by separating said p-type semiconductor substrate having said first semiconductor layer through said separation layer.

[0029] A process for manufacturing a semiconductor wafer according to the present invention comprises the steps of:

forming at least a first semiconductor layer comprising an epitaxial semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of a p-type semiconductor substrate; and a second semiconductor layer comprising an epitaxial semiconductor layer having impurity concentration, which defines p-type conductivity, higher than that of said first semiconductor layer; arranged on said p-type semiconductor substrate in the order as mentioned; making said second semiconductor layer and part of said first semiconductor layer porous; and forming a third semiconductor layer onto said second semiconductor layer made porous; thereby forming a first member; and
transferring said third semiconductor layer onto said second member to form a first semiconductor wafer, and forming a second semiconductor wafer comprising said p-type semiconductor substrate having said first semiconductor layer.

[0030] A method for using a semiconductor wafer according to present invention is characterized by preparing a seed-wafer which has been used for manufacturing a bonded SOI substrate followed by conducting smoothing treatment on at least one surface of said seed-wafer so as to be sold as a semiconductor wafer without being used for

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manufacturing the bonded SOI substrate again.

BRIEF DESCRIPTION OF THE DRAWINGS

[0031] FIG. 1 is a flow chart showing a process for manufacturing a semiconductor wafer according to a fundamental, embodiment of the present invention.

[0032] FIG. 2 is a flow chart showing a process for manufacturing a semiconductor wafer according to another fundamental embodiment of the present invention.

[0033] FIG. 3 is a flow chart showing a process for manufacturing a semiconductor wafer according to another fundamental embodiment of the present invention.

[0034] FIGS. 4A, 4B, 4C, 4D, 4E, 4F and 4G are process diagrams showing a process for manufacturing a wafer according to a first embodiment of the present invention.

[0035] FIGS. 5A, 5B, 5C, 5D, 5E, 5F, 5G, 5H and 5I are process diagrams showing a process for manufacturing a wafer according to a second embodiment of the present invention.

[0036] FIGS. 6A, 6B, 6C, 6D, 6E, 6F and 6G are process diagrams showing a process for manufacturing a wafer according to a fourth embodiment of the present invention.

[0037] FIGS. 7A, 7B, 7C, 7D, 7E, 7F, 7G, 7H and 7I are process diagrams showing a process for manufacturing a wafer according to a fifth embodiment of the present invention.

[0038] FIGS. 8A, 8B, 8C, 8D, 8E, 8F and 8G are process diagrams showing a process for manufacturing a wafer according to a seventh embodiment of the present invention.

[0039] FIGS. 9A, 9B, 9C, 9D, 9E, 9F and 9G are process diagrams showing a process for manufacturing a wafer according to an eighth embodiment of the present invention.

[0040] FIG. 10 is an explanatory diagram showing an example of a manufacturing system.

[0041] FIG. 11 is an explanatory diagram showing another example of a manufacturing system.

[0042] FIG. 12 is a flow chart of an inspection process for determining use to which a first wafer after separation is diverted.

[0043] FIG. 13 is an explanatory diagram showing an example of a manufacturing system.

[0044] FIG. 14 is an explanatory diagram showing another example of a manufacturing system.

[0045] FIGS. 15A, 15B, 15C, 15D, 15E, 15F, 15G and 15H are process diagrams showing a process for manufacturing a wafer of the present invention.

[0046] FIGS. 16A, 16B, 16C and 16D are process diagrams showing a process for manufacturing a solar battery of the present invention.

[0047] FIGS. 17A, 17B, 17C, 17D and 17E are schematic diagrams showing a prior art process for transferring an epitaxial layer.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0048] FIG. 1 is a flow chart showing a process for manufacturing a semiconductor wafer according to a fundamental embodiment of the present invention.

[0049] First, as shown in step S1 of FIG. 1, a semiconductor wafer is provided as a first wafer. As a semiconductor wafer, both an SOI wafer and a non-SOI wafer can be employed. In particular, non-SOI wafers such as a CZ wafer, an FZ wafer, an epitaxial wafer, and a hydrogen-annealed wafer are preferably employed. The CZ wafer and FZ wafer are wafers produced by the Czochralski process and floating zone process, respectively.

[0050] Next, as in step S2, a separation layer is formed on the semiconductor wafer, and a first member having a monocrystalline semiconductor on a semiconductor substrate with a separation layer arranged therebetween is formed. There are two methods for forming the separation layer. One is a method for forming a porous layer, and then, forming a non-porous layer on its surface. The non-porous layer is formed by a method of epitaxially growing it on the porous layer, and a method of conducting heat-treatment on the surface of the porous layer in a reducing atmosphere containing hydrogen or the like. The other is a method of injecting at least one ion of a hydrogen ion, a rare gas ion, and a nitrogen ion or the like into the first wafer, thereby forming a layer including fine voids (these fine voids include gas or the like called microbubbles, which are also called micro-cavity) or a layer including potential fine voids that can be produced by subsequent heat treatment at a predetermined depth position from the surface of the first water.

[0051] In any case, a monocrystalline semiconductor layer having its predetermined thickness on the surface of a semiconductor wafer is formed before forming the separation layer, and the separation layer may be formed within the layer.

[0052] A layer on the semiconductor layer is selected from among a monocrystalline semiconductor layer, polycrystalline semiconductor layer, and an amorphous semiconductor layer or the like. Specifically, it includes Si, Ge, SiGe, SiC, C, GaAs, AlGaAs, InGaAs, InP, InAs or the like. Further, on the surface of these semiconductor layers, an insulating

layer such as silicon oxide, silicon nitride, or silicon nitride oxide or the like may be formed by thermal oxidization, CVD, sputtering or the like.

[0053] If a separation layer is not formed in advance, as described later, a multilayer structure may be cut at a proper position after the structure has been formed. Alternatively, if an interface at which stress is produced is prepared, the structure will be separated at the interface. That is, the structure may be via the steps of S1, S3, and S4.

[0054] Then, in step S3, a portion being a support, substrate (a second member) is formed on a semiconductor wafer having a separation layer formed thereon, and a multilayer structure is formed. There are two methods for forming a portion being this support substrate. One is a method of bonding an additionally provided second wafer on the first wafer having the separation layer formed thereon; and the other is a method of depositing a relatively thick material such as polycrystalline silicon on the first wafer, thereby forming a support substrate. As a second wafer, a wafer having the same structure as the first semiconductor substrate such as a CZ wafer, an FZ wafer, an epitaxial wafer, a hydrogen annealed wafer or the like can be employed. The first wafer may be bonded directly on the semiconductor surface of these wafers or may be bonded via an insulating layer and/or a bonding layer between these wafers. Alternatively, in place of the second wafer, an insulating transparent substrate such as quartz glass, plastics or the like, a conductive metal substrate such as flexible metal film, aluminum, stainless steel or the like, or ceramics or the like can be employed, and the first wafer may be bonded directly or indirectly thereto via the insulating layer and/or the bonding layer.

[0055] Then, in step S4, a multilayer structure is separated on the separation layer. There are two separation methods. One is a method of externally heating a multilayer structure, emitting light to the multilayer structure to absorbe light, thereby generating separation energy inside of the multilayer structure. Specifically, a layer including fine voids formed by implanting a hydrogen ion, a rare gas ion, a nitride ion or the like at a predetermined depth position of the first wafer or a layer including potential fine voids is subjected to thermal energy, whereby its density decreases with increasing the fine voids. In this manner, a release phenomenon of a multilayer structure occurs in the layer. This is a method of generating separation energy inside the multilayer structure. Alternatively, there may be a separation method of oxidizing the separation layer and/or its vicinity from the side by heating process and utilizing stress due to growth of oxide film or the like. The above heat energy is generated by heat treatment at 300°C to 800°C or preferably heat treatment at 400°C to 600°C.

[0056] The other is a method of externally imparting separation energy directly to a multilayer structure. Specifically, it includes a method of inserting a wedge into the side of the multilayer structure, thereby peeling the structure; a method of blowing a fluid consisting of liquid and/or gas on the side of the multilayer structure, thereby peeling the structure; a method of applying tensile force in opposite directions to the front and back surfaces of the multilayer structure with each other, thereby peeling the structure; a method of applying a pressing force in opposite directions to the front and back surfaces of the multilayer structure with each other, thereby destroying to peel a separation layer; a method of applying shear force to the side of the multilayer structure, thereby destroying the separation to peel the structure; a slicing method using an inner circumference blade or a wire saw; or a method of imparting ultrasonic wave vibration, thereby destroying the separation layer and the like.

[0057] As for a fluid to be used, there can be used an organic solvent such as alcohol without using water; acid such as hydrofluoric acid and nitric acid; or alkali such as potassium hydroxide; and liquid having function of selectively etching the other separation area or the like. Further, as a fluid, gas such as air, nitrogen gas, carbonic acid gas, rare gas or the like may be employed. Gas or plasma capable of etching action to the separation area can be employed. For use as jet flow, it is desirable to use water with its high purity such as pure water or ultra-pure water having impurity metal or particles removed therefrom. However, when the separation step is carried out in a completely low-temperature process, it is possible to perform rinsing and removal after water jet separation.

[0058] Of course, the above mentioned various separation methods may be used in combination.

[0059] The thus obtained wafer becomes a highly value-added wafer such as an SOI wafer, and a semiconductor device is produced using the wafer. The produced semiconductor device has its superiority in low power consumption, and can be operated at high speed (step S5).

[0060] On the other hand, the separated first wafer (semiconductor substrate) is employed as a non-SOI wafer with its surface being smoothed (smoothened) instead of being utilized as a first or second wafer again in the above step, and a general semiconductor device is provided by utilizing the wafer.

Alternatively, this wafer can be used as a monitoring or dummy wafer (step S6). In addition, the wafer can be diverted for producing solar cells through a process disclosed in Japanese Patent Application Laid-Open Nos. 8-213645, 10-233352, and 10-270361.

[0061] For surface smoothing, at least one out of polishing, grinding, etching, heat treatment or the like may be applied to the separated first wafer. In particular, a method of conducting heat treatment on the first wafer separated in a reducing atmosphere containing hydrogen (hydrogen annealing) is a more preferred method in that surface smoothing is made possible while a decrease in wafer thickness is suppressed, and at the same time, impurities such as boron contained in the wafer surface layer after separation are diffused outwardly, making it possible to lower the concentration of impurities.

[0062] A temperature preferable for hydrogen annealing is above 300°C and below the melting point of a wafer-consisting material. When this annealing is applied to a monocrystalline silicon wafer, the lower limit of the temperature is 800°C, more preferably 1000°C, and the upper limit of the temperature is the melting point of the silicon, more preferably 1400°C, or further preferably 1200°C.

[0063] The pressure of a reducing atmosphere preferable to hydrogen annealing may be increased pressure, atmospheric pressure, or reduced pressure, it should be below the atmospheric pressure and 3.9×10^4 Pa or above, or it should be preferably below the atmospheric pressure and 1.3 Pa or more.

[0064] The treatment time preferable to hydrogen annealing is not particularly limited, because it is selected appropriately according to required properties. The realistic range is from about 1 minute to 10 hours.

[0065] As a gas for providing a reducing atmosphere containing hydrogen, 100% hydrogen and a mixture gas of hydrogen and inert gas can be employed.

[0066] A first wafer after peeling, which was obtained via such hydrogen annealing, is at the same level as that of a commercially available hydrogen-annealed wafer, which is preferable to produce a semiconductor device such as LSI.

[0067] Smoothing due to polishing is a very superior method. Even if a surface failure occurs, the faulty surface can be almost removed by polishing it. Unlike surface polishing of the SOI layer, severe requirements are not applied to this polishing with respect to its uniformity. The polishing can be performed by a method similar to polishing of a general Si wafer, and is superior in mass productivity. However, the wafer thickness is decreased by polishing, and thus, hydrogen annealing is superior in this point of view.

[0068] As a polishing method, chemical and mechanical polishing (CMP) is preferred. As a polishing agent for performing CMP, there can be employed silica glass (borosilicate glass), titanium dioxide, titanium nitride, aluminum oxide, iron nitrate, cerium oxide, colloidal silica, silicon nitride, silicon carbide, graphite, polishing granule such as diamond, or a granule liquid having these granules and oxidizing agent such as H_2O_2 or KIO_3 or alkali solution such as NaOH, KOH or the like mixed therewith.

[0069] Smoothing or smoothening steps can be omitted. Of course, in the case of polishing, mirror face polishing may be carried out or not only one side but also both sides may be mirror-face polished.

[0070] In the present invention, when a P-type semiconductor wafer is employed as a first wafer in particular, as shown in FIG. 2, a first semiconductor wafer such as an SOI wafer is prepared (step S5) in separation step S4; the separated P-type semiconductor wafer is smoothed, a P^- layer or an N layer and the like is epitaxially grown (step S6) on its surface; and then an epitaxial wafer having a P^- layer or an N layer and the like formed on a P-type semiconductor wafer can be prepared (step S7). In particular, as a P-type semiconductor wafer, a high concentration P-type semiconductor wafer is preferably employed. This is because, as described later, in particular, the form of P^- epitaxial/P^+ substrate is the most widely employed among the currently employed wafer. Epitaxial growth treatment may be applied after the surface of the first wafer after peeling has been once smoothened. This epitaxial growth treatment can be applied after only rinsing after peeling without applying polishing, etching, or heat treatment.

[0071] When an epitaxial semiconductor layer is formed on a high condensed P-type semiconductor wafer as a first wafer, and is employed, as shown in FIG. 3, a first semiconductor wafer such as an SOI wafer is prepared (step S5) in separation step S4. In addition, an epitaxial semiconductor layer remains on the separated high concentration P-type semiconductor wafer depending on a separation position. Thus, an epitaxial wafer can be prepared without newly causing epitaxial growth (step S7). For example, an epitaxial wafer having P^- epitaxial layer is completed on the P^+ substrate. That is, an epitaxial semiconductor layer is formed in step S1, on which a separation layer is formed. Thus, unlike FIG. 2, there is no need for providing a new epitaxial semiconductor layer in step S6. In particular, a P^-- (or N-) type first semiconductor layer is formed on the high concentration P-type semiconductor wafer, on which a second semiconductor layer is further formed, and the separation position is preferably provided inside of the first semiconductor layer. The high concentration P type has a boron concentration of 1×10^{17} cm^{-3} to 1×10^{20} cm^{-3} and a specific resistance of 0.001 to 0.5 ohm.cm resistance.

[0072] Making it porous for forming a separation layer is conditionally possible on a N-type semiconductor, and however, it is desirable to employ a P-type semiconductor. Unagami et al. studied Si solution reaction in anodization, and concluded that positive pores were required in anodization in HF solution (T Unagami, J. Electrochem. Soc., vol. 127,476 (1980)). To make it porous, a high concentration P-type semiconductor wafer is preferably employed, and its impurities concentration range is generally from $5.0 \times 10^{16}/cm^3$ to $5.0 \times 10^{20}/cm^3$, preferably $1.0 \times 10^{17}/cm^3$ to $2.0 \times 10^{20}/cm^3$, and more preferably, $5.0 \times 10^{17}/cm^3$ to $1.0 \times 10^{20}/cm^3$. When a separation layer is formed by ion plantation, hydrogen, nitrogen, rare gas or the like (He, Ne, Ar or the like) is employed as an ion implantation species. At least one or more of them may be implanted.

[0073] A temperature preferable to epitaxial growth is 500°C or above and below the melting point of a wafer-consisting material. When epitaxial growth is applied to a monocrystalline silicon wafer, the lower limit of temperature is 600°C, more preferably 800°C, and the upper limit of the temperature is the melting point of the silicon, more preferably 1400°C, and further preferably 1200°C.

[0074] Epitaxial growth is carried out by CVD method or sputtering method, the preferable atmospheric pressure

may be atmospheric pressure or reduced pressure, should be below atmospheric pressure and 3.9×10^{-4} Pa or more, or should be more preferably below atmospheric pressure and 1.3 Pa or above.

[0075] The treatment time preferable to epitaxial growth is not limited in particular, because it is selected according to a required film thickness. The realistic range is from 10 seconds to 10 hours.

[0076] As an atmospheric raw material gas for epitaxial growth, there is exemplified at least one gas selected from among silane or its analogous such as SiH_4, $SiCl_3H$, $SiCl_2H_2$, $SiCl_4$, Si_2H_6, SiF_4 or the like. For the purpose of addition of impurities, acceptor-containing gas such as B_2H_6, BF_3, BBr_3 or donor-containing gas such as PH_3, AsH_3 or the like may be added thereto. Further, hydrochloric acid, chlorine or the like may be added to the above or hydrogen or rare gas may be added. In general, hydrogen gas is employed as a carrier gas.

[0077] As described above, in one embodiment of the present invention, an SOI wafer is fabricated using a P^+ wafer preferable to make it porous as a first wafer, and an epitaxial layer is grown on the surface of the first wafer after peeling, and the epitaxial wafer is produced. The produced epitaxial wafer is preferable to produce integrated circuits such as memory, logic circuit, analog signal processing circuit, and analog-digital hybrid circuit or semiconductor functional elements such as CCD, solar cells or the like. In a single manufacturing process, both of the SOI wafer and epitaxial wafer can be manufactured, and comprehensive material cost can be reduced.

[0078] Hereinafter, an epitaxial wafer will be described.

[0079] In low power consumption and high-speed LSI technology (Realize Co., Ltd., P. 479 to P. 483), as one of the substrate structures for reducing a digital noise, a P^- epitaxial layer/P^+ substrate is exemplified.

[0080] According to Section 5-1, Silicon Science (UCS Semiconductor Substrate Technical Study Society, Realize Co., Ltd.), when a MOS LSI is manufactured on an epitaxial wafer, most of the MOS LSI is employed in the P-type epitaxial/P^+ substrate structure. Thus, the most important factor for which the epitaxial wafer is employed is that a software error and a latch-up can be improved. In addition, in Section 5.4, the epitaxial wafer of the P-type epitaxial/P^+ substrate has its TDDB characteristics better than the CZ bulk Si wafer in insulation breakage characteristics of the MOS-structured oxide film, and there is a strong getting effect due to the region high in boron concentration in the substrate.

[0081] In this section, the price of an epitaxial wafer is discussed. If the aperture of the wafer becomes large, the difference in price between the epitaxial wafer and the CZSi wafer becomes small. For a gigabit age, an ultra-high quality Si crystal is required. Further, there comes an age in which a large amount of epitaxial wafers are used for highly integrated MOS LSI such as DRAM due to an increase in price ratio (against epitaxial wafer price) of the CZ crystal which has a larger diameter.

[0082] In the present invention, when a porous layer is formed as a separation layer, a high concentration P^+ wafer is desirably employed. When the separated high concentration p^+ wafer (semiconductor substrate) is utilized or diverted as a P^--epitaxial substrate without discarding it, one high-quality SOI wafer and one epitaxial wafer can be manufactured from these two wafers. In addition, as a wafer for manufacturing an SOI wafer, a new wafer can be always employed, and thus, the SOI wafer manufacturing efficiency can be increased. Therefore, a commercially advantageous semiconductor production system can be constructed for mass-consumption of the above mentioned epitaxial wafer.

[0083] When P^- wafer is employed as a first wafer, a wafer preferable to produce the above mentioned integrated circuit or semiconductor functional element is formed merely by smoothing the surface without applying epitaxial growth treatment. Of course, when a higher quality layer is required for producing such integrated circuit or semiconductor functional element, an epitaxial layer may be further formed on the smoothed surface. When the separated first wafer (semiconductor substrate) is utilized or diverted, the price of this wafer is almost equal to or more inexpensive than the initial wafer. Further, if the wafer is highly value-added, it can be sold at a higher price, and thus, a commercially advantageous semiconductor production system can be constructed.

[0084] Hereinafter, preferred embodiments of the present invention will be described in more detail with reference to the accompanying drawings.

(Embodiment 1)

[0085] FIGS. 4A to 4G are schematic views showing a wafer manufacturing process according to a First Embodiment of the present invention.

[0086] First, as shown in FIG. 4A, the surface of a first wafer 1 consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like is subjected to a nodization to make it porous, and a porous layer 4 is formed.

[0087] Then, as shown in FIG. 4B, a non-porous layer 5 is formed on the porous layer 4 to form a first member. A method for forming the non-porous layer 5 includes hydrogen annealing to close the pores of the porous layer 4 so as to make it non-porous or forming a non-porous monocrystalline layer by epitaxial growth. In addition, the surface of the non-porous layer 5 is oxidized as required, thereby forming an insulating layer 6 on the non-porous layer 5. Instead of oxidization, the insulating layer 6 may be formed by CVD or sputtering and the like. In this embodiment, a porous layer 4 is employed as a separation layer.

[0088] As shown in FIG. 4C, the surface of an insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multilayer structure.

[0089] The second wafer 2 may be a wafer on which a semiconductor is exposed or may have an insulating film formed on its surface. Alternatively, instead of the second wafer, an insulating light transmission substrate such as quartz glass may be employed. Alternatively, a plastic-based flexible film may be employed.

[0090] In this bonding, the surfaces of these wafers may be subjected to heat treatment in contact with each other at room temperature to increase bonding strength, and may be bonded with each other by anode bonding. Alternatively, heat treatment may be carried out at the same time as when they come into contact with each other. Further, in the bonding step, heat treatment or the like may be carried out while they are pressurized so as to come into closer contact with each other. Heat treatment is preferably carried out in an oxidizing atmosphere or an inert gas atmosphere (N_2, Ar or the like).

[0091] In addition, it is preferable to activate a bonding face in advance by applying plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least either one of a pair of bonding faces. Further, a bonding layer may be intervened between these faces for bonding.

[0092] As shown in FIG. 4D, at a separation layer (porous layer 4), a multilayer structure is separated by the aforementioned method (reference numerals 41 and 42 each designate a separated porous layer). A non-porous portion of the peeled first wafer 1 is maintained to a wafer shape, and a remaining portion 41 of the porous layer is provided on a separated face. On the other hand, a non-porous layer 5 transferred from the first wafer is provided on the second wafer 2 together with the insulating layer 6. A remaining portion 4B of the porous layer is provided on its separated face. On the drawing, although the separation position is drawn so as to be inside of the porous layer, of course, an interface between the first wafer 1 and the porous layer 4 or an interface between the non-porous layer 5 and the porous layer 4 may be at the separation position. This is the same in the subsequent embodiments.

[0093] As shown in FIG. 4E, a remaining portion 42 of the porous layer is removed. When the thickness of the remaining portion 42 is relatively thick, a mixture liquid of fluoric acid, hydrogen peroxide, and alcohol is employed as an etchant, the remaining portion 42 is selectively removed by wet etching, and then, the surface is smoothened by hydrogen annealing. If the thickness of the remaining portion 42 is thin, the remaining portion 42 may be removed by hydrogen annealing without wet etching, and at the same time, smoothing treatment may be carried out. Thus, a highly value-added SOI wafer is obtained. The polishing or planing step may be added to the removing step of the remaining portion 42.

[0094] In FIG. 4F, the remaining portion 41 on the wafer 1 (semiconductor substrate) after peeling is removed, smoothed, and smoothened by polishing, planing, wet etching, or hydrogen annealing and the like. Thus, a bulk wafer is obtained. Here, on the first wafer on which the remaining portion 41 has been merely removed, i.e., on which the remaining portion 41 has been removed without smoothing its surface, epitaxial growth (FIG. 4G) may be carried out for the surface smoothing step.

[0095] As shown in FIG. 4G, an epitaxial layer 7 consisting of a non-porous P-type monocrystalline semiconductor may be formed by carrying out epitaxial growth treatment on the surface of the wafer 1 after peeling. Thus, an epitaxial wafer is obtained. That is, one SOI wafer (FIG. 4E) and one bulk wafer (FIG. 4F) or an epitaxial wafer (FIG. 4G) are obtained from two semiconductor wafers. In the present invention, this bulk wafer (epitaxial wafer) is employed for uses other than the aforementioned first and second wafers. For example, the wafer is used for fabricating a solar cell, is used as a dummy wafer or a monitor wafer, or is for sale as an epitaxial wafer.

[0096] After separation, in the case where a separation layer remaining on the first or second wafer is very thin, there is almost no such layer, or there is no problem even if the layer remains, the step of removing the above remaining portion can be eliminated, which is the same in the subsequent embodiments.

[0097] As has already been described, when a high concentration P-type semiconductor wafer is employed as a first wafer, the wafer is preferable to make it porous. The epitaxial wafer obtained in FIG. 4G is a wafer having an epitaxial layer (for example, P^- layer) formed on the P^+ wafer.

[0098] Here, prior to forming the non-porous layer 5 on the porous layer 4, at least one of the following steps (1) to (4) can be added. A series of steps may be performed in order of (1) → (2) preferably, (1) → (2) → (3) or (1) → (2) → (4) more preferably, and (1) → (2) → (3) → (4) more preferably.

(1) Step of forming a protective layer on the wall of the pores

[0099] A protective film such as oxide film or nitride film may be provided on the wall of the pores in a porous layer to prevent pores from becoming coarse due to heat treatment. For example, heat treatment (200°C to 700°C) is carried out under an oxidizing atmosphere. An oxide film or the like formed on the surface of the porous layer may be removed, as required (for example, a surface is exposed to a liquid containing HF.).

(2) Hydrogen baking step

[0100] A porous layer is subjected to heat treatment at 800°C to 1200°C in a reducing atmosphere containing hydrogen, thereby sealing pores existing on the layer surface of the porous layer to some extent.

(3) Step of supplying a very small amount of raw material

[0101] If pores cannot be sealed by the above hydrogen baking process, a small amount of raw material of the non-porous layer 5 is supplied, thereby further sealing pores on the layer surface.

[0102] Specifically, the supply of the raw material is adjusted so that the growth rate is 20 nm/min. or less, preferably 10 nm,/min. or less, more preferably 2 nm/min. or less.

(4) High-temperature baking step

[0103] Heat treatment is carried out at a temperature higher than a treatment temperature for the aforementioned hydrogen baking step and/or the step of supplying a small amount of raw material and under a hydrogen-containing reducing atmosphere, In this manner, more complete sealing and smoothing on the surface of the porous layer can be achieved.

(Embodiment 2)

[0104] FIGS. 5A to 5I are schematic views showing a method for manufacturing a wafer according to a Second Embodiment of the present invention.

[0105] First, as shown in FIG. 5A, a first wafer 1 consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like is provided; and a dopant-added monocrystalline semiconductor layer 3 is formed on the top layer of the first wafer using a diffusion method or an ion implantation method. This monocrystalline semiconductor layer 3 is preferably a P^+ layer having a boron concentration of 1×10^{17} cm^{-3} to 1×10^{20} cm^{-3}.

[0106] Next, as shown in FIG. 5B, the surface of the monocrystalline semiconductor layer 3 of the first wafer 1 is subjected to anodization to make it porous, and a porous layer 4 is formed. At this time, it is preferable to make only the top layer of the monocrystalline semiconductor layer 3 porous so that a non-porous layer 10 remains below the porous layer 4 with a thickness of about 100 nm to 20 μm. Thus, a region in which the boron concentration is strictly specified can be subjected to anodization, and an evenly porous face can be formed.

[0107] Then, in FIG. 5C, a non-porous layer 5 is formed on a porous layer 4, and a first member is formed. A method for forming the non-porous layer 5 includes closing the pores in the porous layer 4 to make the top layer non-porous by hydrogen annealing or forming a non-porous monocrystalline layer by epitaxial growth. The surface of the non-porous layer 5 is oxidized as required to form an insulating layer 6 on the non-porous layer 5. Instead of heat oxidizing, the insulating layer 6 may be formed by CVD or sputtering and the like. In this embodiment, the porous layer 4 is employed as a separation layer.

[0108] In FIG. 5D, the surface of the insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multilayer substrate. As a second wafer 2, a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like can be employed. The second wafer may be a wafer on which a semiconductor is exposed or may have an insulating layer formed on its surface. Alternatively, an insulating light transmission substrate such as quartz glass may be employed instead of the second wafer.

[0109] In addition, it is preferable to activate in advance a bonding face by applying plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least either one of a pair of bonding faces. Further, a bonding layer may be intervened between these faces.

[0110] In FIG. 5E, at a separation layer (a porous layer 4), a multilayer structure is separated by the aforementioned method. The non-porous portion of the peeled first wafer is maintained to a wafer shape, and has a remaining portion 41 of the porous layer on the separated face. On the other hand, the non-porous layer 5 transferred from the first wafer is provided on the second wafer 2 together with the insulating layer 6, and has a remaining portion 42 of the porous layer on its separated face.

[0111] In FIG. 5F, a remaining portion 42 is removed. When the thickness of the remaining portion 42 is relatively thick, a mixture of hydrofluoric acid, hydrogen peroxide, and alcohol is employed as an etchant, the remaining portion 42 is selectively removed by wet etching, and then, the surface is smoothed by hydrogen annealing. When the thickness of the remaining portion 42 is thin, the remaining portion 42 may be removed by hydrogen annealing without wet etching, and at the same time, smoothing treatment may be carried out. Thus, a highly value-added SOI wafer is obtained.

[0112] In FIG. 5G, the remaining portion 41 on the wafer 1 after peeling (semiconductor substrate) is removed by

polishing, planing, wet etching, hydrogen annealing or the like, and is smoothed.

[0113] In addition, when a non-porous layer 10 is removed, a bulk wafer which is the same as the initial wafer is obtained (FIG. 5H).

[0114] Further, as shown in FIG. 5I, after epitaxial growth treatment has been carried out on the surface of the wafer 1 after peeling, an epitaxial layer 7 consisting of a non-porous P-type monocrystalline semiconductor is formed, and then an epitaxial wafer is obtained. That is, one SOI wafer and one bulk wafer (FIG. 5H) or epitaxial wafer (FIG. 5I) are obtained from two wafers. The bulk wafer (epitaxial wafer) is employed for uses other than the fabrication of the SOI wafer shown in FIGS. 5A to 5I. For example, the wafer is employed as an apparatus wafer for fabricating a solar cell, a MOS transistor or the like, is used as a monitor wafer or a dummy wafer, or is sold as a bulk wafer or an epitaxial wafer.

(Embodiment 3)

[0115] A method for manufacturing a wafer according to a Third Embodiment of the present invention is described below by referring to FIGS. 5A to 5I again.

[0116] First, as shown in FIG. 5A, a first wafer 1 consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like is provided; and a monocrystalline semiconductor layer 3 is formed on its surface by an epitaxial growth treatment. This monocrystalline semiconductor layer 3 is preferably a P^+ layer having a boron concentration of 1×10^{17} cm^{-3} to 1×10^{20} cm^{-3} defining P-type conductivity.

[0117] Next, as shown in FIG. 5B, the surface of the monocrystalline semiconductor layer 3 of the first wafer 1 is subjected to anodization to make it porous, and a porous layer 4 is formed. At this time, it is preferable to make only the top layer of the epitaxial layer 3 porous so that a non-porous epitaxial layer 10 remains below the porous layer 4 with a thickness of about 100 nm to 20 μm.

[0118] Then, in FIG. 5C, a non-porous layer 5 is formed on a porous layer 4, and a first member is formed. A method for forming the non-porous layer 5 includes closing the pores in the porous layer 4 to make the top layer non-porous by hydrogen annealing or forming a non-porous monocrystalline layer by epitaxial growth. The surface of the non-porous layer 5 is oxidized as required to form an insulating layer 6 on the non-porous layer 5. Instead of heat oxidizing, the insulating layer 6 may be formed by CVD or sputtering and the like. In this embodiment, the porous layer 4 is employed as a separation layer.

[0119] In FIG. 5D, the surface of the insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multi-layered substrate. A second wafer 2 consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like may be a wafer on which a semiconductor is exposed or may have an insulating layer formed on its surface. Alternatively, an insulating light transmission substrate such as quartz glass may be employed instead of the second wafer. During the bonding, these surfaces may be subjected to heat treatment in contact with each other at room temperature to increase bonding strength, and may be bonded by anode bonding. Alternatively, heat treatment may be carried out at the same time when these surfaces come into contact with each other. Further, in the bonding step, heat treatment or the like may be carried out while they are pressurized so as to come into closer contact with each other.

[0120] In addition, it is preferable to activate in advance a bonding face by applying plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least either one of a pair of bonding faces.

[0121] Further, a bonding layer may be intervened between these faces.

[0122] In FIG. 5E, at a separation layer (a porous layer 4), a multilayer structure is separated by the aforementioned method. The non-porous portion of the peeled first wafer is maintained to a wafer shape, and has a remaining portion 41 on the porous layer on the separated face. On the other hand, the non-porous layer transferred from the first wafer is provided on the second wafer 2 together with the insulating layer 6, and has a remaining portion 42 of the porous layer on its separated face.

[0123] In FIG. 5F, a remaining portion 42 is removed. When the thickness of the remaining portion 42 is relatively thick, a mixture of hydrofluoric acid, hydrogen peroxide, and alcohol is employed as an etchant, the remaining portion 42 is selectively removed by wet etching, and then, the surface is smoothed by hydrogen annealing. When the thickness of the remaining portion 42 is thin, the remaining portion 42 may be removed by hydrogen annealing without wet etching, and at the same time, smoothing treatment may be carried out. Thus, a highly value-added SOI wafer (FIG. 5F) is obtained.

[0124] In FIG. 5G, the remaining portion 41 on the wafer 1 after peeling (semiconductor substrate) is removed by polishing, wet etching, hydrogen annealing or the like, and is smoothened. At this time, the epitaxial layer 10 formed in FIG. 5A remains. When hydrogen annealing is applied in this state, the surface is smoothened. In addition, the concentration of boron contained is lowered by outward diffusion, and the layer 10 is formed as a P^- type monocrystalline semiconductor layer. This is a wafer of the same quality as a so-called P^- epitaxial wafer. If there is no need for positively conducting outward diffusion, even if the surface is smoothed by polishing or short-time hydrogen annealing, a wafer

of the same quality as the P⁻ epitaxial wafer is formed. An epitaxial layer may be epitaxially grown on the layer 10.

[0125] In addition, when the layer 10 is removed, a bulk wafer which is the same as the initial wafer is obtained (FIG. 5H).

[0126] Further, as shown in FIG. 5I, after epitaxial growth treatment has been carried out on the surface of a wafer 1 after peeling, an epitaxial layer 7 consisting of a non-porous P-type monocrystalline semiconductor is formed as an epitaxial wafer. That is, one SOI wafer and one epitaxial wafer or bulk wafer are obtained from two wafers. This non-SOI wafer is diverted or is sold for other use without being used for manufacturing an SOI wafer again.

[0127] Hereinafter, an advantage in the case where one SOI wafer and one epitaxial wafer is fabricated from two silicon wafer will be described with reference to FIG. 15A to FIG. 15H.

[0128] As shown in FIG. 15A, an epitaxial silicon layer 3 is formed on a bulk silicon substrate 1.

[0129] Next, as shown in FIG. 15B, a part of the epitaxial layer 3 is subjected to anodization, thereby making it porous, and a porous layer (a separation layer) 4 is formed. Then, a non-porous monocrystalline silicon layer 5 being an active layer of the SOI wafer is formed on the porous layer 4 (FIG. 15C). Further, an oxide film 6 being a part of the insulating film of the SOI wafer is formed (FIG. 15D). At this time, as shown in the figure, an oxide film is also formed on the surface of the silicon substrate 1. A second silicon wafer 2 is bonded thereto (FIG. 15E). In this bonding, heat treatment may be carried out at an oxidizing atmosphere so that bonding force is strengthened, and the oxide film on the surface of the silicon substrate 1 can be thickened as well. Thereafter, the bonded substrates are separated (FIG. 15F), the remaining porous layers 41 and 42 are removed, thereby making it possible to obtain a SOI wafer (FIG. 15G) and an epitaxial wafer (FIG. 15H).

[0130] In the process step, an epitaxial wafer for forming an apparatus is employed in order to prevent diffusion of impurities from the wafer to the outside while an oxide film being a back shield is attached to the surface, in particular, to the back face of the substrate.

[0131] According to the aforementioned step, even if the step of forming a back shield discriminated from the other step is not provided, such back shield is formed in a series of the steps of fabricating the SOI wafer. Thus, an epitaxial wafer can be fabricated very effectively.

[0132] In particular, the thickness of the back surface oxide film of the epitaxial wafer (FIG. 15H) obtained through a series of SOI wafer fabricating steps is preferably controlled to be 10 nm to 10 μm, and more preferably 100 nm to 3 μm.

[0133] In FIGS. 15A to 15H, a case in which anodization is employed to form a separation layer has been described. When an SOI wafer is fabricated utilizing a microbubble layer formed by ion implantation, an epitaxial wafer with a back shield can be obtained at the same time as the separation step by containing two oxidizing steps (the oxidizing step of forming a protective film on the surface of a silicon wafer prior to ion implantation and the oxidizing step for increasing bonding strength).

(Embodiment 4)

[0134] FIGS. 6A to 6G are schematic views showing a wafer manufacturing method according to a Fourth Embodiment of the present invention.

[0135] First, in FIG. 6A, a first wafer consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like is provided. The surface of the first wafer is oxidized as required, thereby forming an insulating layer 6. Then, in FIG. 6B, an ion selected from hydrogen, nitrogen, and rare gas is implanted, a layer 14 containing fine cavities (micro bubbles or micro-cavities) being a separation layer is formed at a predetermined depth. Thus, a first member having a non-porous layer 5 of monocrystalline semiconductor is formed on the separation layer 14.

[0136] In FIG. 6C, the surfaces of the insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multilayer structure. The second wafer may be a wafer on which a semiconductor is exposed, and may have an insulating film such as oxide film formed on its surface. Alternatively, an insulating light transmission substrate such as quartz glass may be employed instead of the second wafer. This bonding may be carried out at room temperature. During the bonding, these surfaces may be subjected to heat treatment in contact with each other at room temperature to increase bonding strength, and may be bonded by anode bonding. Alternatively, heat treatment may be carried out at the same time when these surfaces come into contact with each other. Further, in the bonding step, heat treatment or the like may be carried out while they are pressurized so as to come into closer contact with each other. In addition, a bonding layer is intervened between these surfaces to be bonded. Further, it is also preferable to carry out plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least one of a pair of bonding faces, thereby activating the bonding face in advance.

[0137] As shown in FIG. 6D, at the separation layer 14, a multilayer structure is separated using the aforementioned method. In this method, when a temperature is set to 400°C or above during heat treatment in FIG. 6C, a separation phenomenon can occur at the same time as bonding. Preferably, the temperature ranges from 400°C to 600°C.

[0138] The non-porous portion of the peeled first wafer is maintained to a wafer shape, and has a remaining portion 141 of the separation layer 14 on the separated face. On the other hand, on the second wafer 2, the non-porous layer

5 transferred from the first wafer is provided together with an insulating layer 6, and has a remaining portion 142 of the separation layer 14 on the separated face.

[0139] In FIG. 6E, the remaining portion 142 is removed. At this time, the portion may be polished at a low polishing rate, and then, may be subjected to hydrogen annealing. Alternatively, hydrogen annealing may be carried out without polishing the remaining portion 142 to remove it, and at the same time, smoothing treatment may be carried out. Thus, a highly value-added SOI wafer is obtained.

[0140] In FIG. 6F, the remaining portion 141 on the wafer 1 (semiconductor substrate) after peeling is removed by polishing, wet etching, hydrogen annealing or the like, and is smoothed. Thus, a bulk wafer is obtained. Further, as shown in FIG. 6G, epitaxial growth treatment may be carried out on the surface of the wafer 1 after peeling as required, thereby forming an epitaxial layer 7 consisting of a non-porous P-type monocrystalline semiconductor. In this case, an epitaxial wafer is obtained.

[0141] A high concentration P-type wafer is employed as a first wafer 1, and P^- monocrystalline layer is employed as an epitaxial layer 7, thereby forming a P^- epitaxial/P^+ substrate shown in FIG. 6G. In FIG. 6E, when hydrogen annealing is carried out, the high concentration P^+ layer 5 gives an SOI wafer (P^- layer) of low concentration by outward boron diffusion. The P^- epitaxial/P^+ substrate is diverted to various uses other than the aforementioned SOI wafer fabrication.

(Embodiment 5)

[0142] FIGS. 7A to 7I are schematic views showing a method for manufacturing a wafer according to a Fifth Embodiment of the present invention.

[0143] First, as shown in FIG. 7A, a first wafer 1 consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like is provided; and a monocrystalline semiconductor layer 3 is formed on the surface using an epitaxial growth treatment.

[0144] Next, as shown in FIG. 7B, the surface of the epitaxial layer 3 of the first wafer 1 is oxidized as required, thereby forming an insulating layer 6 (FIG. 7B). Then, an ion selected from hydrogen, nitrogen, and rare gas is implanted, so that a layer 14 containing fine cavities being a separation layer is formed at a predetermined depth. Thus, a non-porous layer 5 of monocrystalline semiconductor remains on the separation layer 14, thereby forming a first member (FIG. 7C).

[0145] At this time, an ion is preferably implanted into the epitaxial layer 3 so that a non-porous epitaxial layer 10 remains below the separation layer 14 with a thickness of about 10 nm to 20 μm.

[0146] In FIG. 7D, the surface of the insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multilayer substrate. A second wafer 2 being a second member consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like may be a wafer on which a semiconductor is exposed or may have an insulating layer formed on its surface. Alternatively, an insulating light transmission substrate such as quartz glass may be employed instead of the first wafer. This bonding may be carried out at room temperature. During the bonding, heat treatment may be carried out while these surfaces come into contact with each other at room temperature to increase the bonding strength, and they may be bonded by anode bonding. Alternatively, heat treatment may be carried out at the same time when they come into contact with each other. Further, in the bonding step, heat treatment or the like may be carried out while these surfaces are pressurized to come into closer contact with each other. A bonding layer may be intervened between these surfaces to be bonded. In addition, it is preferable to activate in advance a bonding face by applying plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least either one of a pair of bonding faces.

[0147] In FIG. 7E, at a separation layer 14, a multilayer porous structure is separated by the aforementioned method. When a temperature is set to 400°C to 600°C at the time of heat treatment in step S43, a separation phenomenon will occur at the same time as bonding.

[0148] The peeled first wafer 1 is maintained to a wafer shape without a decrease in its thickness, and has a remaining portion 141 of the separation layer 14 on the separated face. On the other hand, the non-porous layer 5 transferred from the first wafer is provided on the second wafer 2 together with the insulating layer 6, and has a remaining portion 142 of the separation layer 14 on its separated face. In FIG. 7F, a remaining portion 142 is removed. At this time, polishing may be conducted at a low polishing rate, and then hydrogen annealing may also be conducted. Alternatively, hydrogen annealing may be conducted without polishing, and smoothing treatment may be conducted with removing the remaining portion 142. Thus, a highly value-added SOI wafer is obtained.

[0149] In FIG. 7G, the remaining portion 141 on the wafer 1 after peeling (semiconductor substrate) is removed by polishing, wet etching, hydrogen annealing or the like, and is smoothed. At this time, the epitaxial layer 10 formed in FIG. 7C remains. When hydrogen annealing is applied in this state, the surface is smoothened. In addition, if the boron concentration is high, the concentration of boron contained is lowered by outward diffusion, and the layer 10 is formed as a P^- type monocrystalline semiconductor layer.

[0150] In addition, when the epitaxial layer 10 is removed, a bulk wafer which is the same as the initial wafer is obtained (FIG. 7H).

[0151] Further, as shown in FIG. 7I, after epitaxial growth treatment has been carried out on the surface of a wafer 1 after peeling, an epitaxial layer 7 consisting of a non-porous P-type monocrystalline semiconductor may be formed. Thus, an epitaxial wafer is obtained. That is, one SOI wafer and one bulk wafer or epitaxial wafer are obtained from two wafers. In the present invention, the non-SOI wafer is employed for uses other than fabrication of the SOI wafer.

[0152] A high concentration P-type wafer is employed as a first wafer 1, and a P^- monocrystalline layer is employed as an epitaxial layer 7, thereby causing a P^- epitaxial/P^+ substrate to be formed in step S47. In step S45, when hydrogen annealing is carried out, the high concentration P^+ layer 5 gives an SOI wafer (Player) of low concentration by outward boron diffusion.

(Embodiment 6)

[0153] As a first substrate, a semiconductor substrate such as a silicon wafer is employed. On the semiconductor substrate, a semiconductor layer consisting of a material different from that of a hetero-epitaxially grown substrate is formed by CVD or molecular-beam epitaxial growth method. This semiconductor is SiGe or Ge.

[0154] On the other hand, as a second substrate, a silicon wafer is employed.

[0155] An insulating film such as an oxide film is formed on at least one of the surface of the semiconductor layer and/or the surface of the second substrate.

[0156] The first and second substrates are bonded with each other, and a multilayer structure is obtained.

[0157] In the thus obtained multilayer structure, a stress is concentrated on a hetero interface, i.e., an interface between the first substrate and the semiconductor layer, and thus, the multilayer structure is easily peeled at this interface.

[0158] Therefore, when energy is applied for the above mentioned separation, it triggers separation of the multilayer structure, and the semiconductor layer is transferred onto the second substrate. The separation face may be somewhat reeled, and smoothing is carried out as required. Thus, one SOI wafer and one silicon wafer (or epitaxial wafer if epitaxial growth is carried out thereon) can be obtained from two silicon wafers. The thus obtained silicon wafer is employed for uses other than the above mentioned step, whereby making it possible to employ always a new silicon wafer for SOI wafer fabrication.

(Embodiment 7)

[0159] FIGS. 8A to 8G are schematic views showing a wafer manufacturing method according to a Seventh Embodiment of the present invention.

[0160] First, in FIG. 8A, a first wafer 1 consisting of a P-type silicon wafer is employed. Then, an epitaxial layer 31 having its impurity concentration lower than the first wafer and an epitaxial layer 32 having its impurity concentration higher than the epitaxial layer 31 are formed by epitaxial growth. For a P-type silicon wafer, a high concentration P-type silicon wafer of 1×10^{17} cm^{-3} to 1×10^{20} cm^{-3} in boron concentration and 0.001 to 0.5 Ω·cm in specific resistance is preferred.

[0161] The impurity concentration of the epitaxial layer 32 is required to be higher than that of the epitaxial layer 31. The specific resistance of the epitaxial layer 32 is set to be lower than that of the epitaxial layer 31. Specifically, the specific resistance of the epitaxial layer 31 is set to be 0.02 to 10,000 Ω·cm, and more preferably 0.1 to 100 Ω·cm. The specific resistance of the epitaxial layer 32 is set to be 0.001 to 0.1 Ω·cm, and more preferably 0.005 to 0.02 Ω·cm.

[0162] In FIG. 8B, the epitaxial semiconductor layer 32 and epitaxial layer 31 of the first wafer 1 is subjected to anodization partway, thereby making them porous, and a porous layer 4 is formed. Even if a current is constant during anodization, when epitaxial layers having their different impurity concentrations are thus employed, a porous layer having its different degree of porousness can be formed. In the porous layer 4, the porous portion of the epitaxial semiconductor layer 31 is more highly porous and more vulnerable than that of the semiconductor layer 32. At this time, the layer is made porous so that the non-porous layer 10 remains below the porous layer 4 with a thickness of 100 nm to 20 μm.

[0163] Hereinafter, forming an epitaxial layer having its different impurity concentration will be described in more detail.

[0164] At least one of the composition, impurity concentration, and type of an epitaxially grown layer is changed, (in this embodiment, impurity concentration was changed), thereby forming a structure having two or more epitaxially grown layers. When a porous layer formed in such epitaxially grown layer is structured to be porous, the layer having two or more layers having their different structures, a separation position in the porous layer can be specified in the post-bonding separation step described later.

[0165] It is desirable that a porous layer structure has a lowly porous layer on its surface side and a highly porous

layer therein. The lowly porous layer on the surface side is required to improve crystallinity of a non-porous monocrystalline layer to be formed later. The highly porous layer positioned therein is a layer that is mechanically vulnerable and that is preferentially separated mainly in the highly porous layer or at an interface between the highly porous layer and the adjacent layer in the separation step.

[0166] Prior to forming the porous layer, a layer having different composition, impurity concentration, type or the like from the above is formed in advance in an epitaxially grown layer, whereby at least the above mentioned lowly and highly porous layers can be formed without particularly changing the conditions for forming a porous layer during anodization for forming the porous layer.

[0167] When a plurality of first substrates are disposed in an anodization solution to form a porous layer, a silicon wafer has been disposed on the anode side as a shield wafer in order to prevent the deposition of a metal ion eluted from the anode to the back side of the first substrate. When two or more porous layers are formed by changing a current density, a similar structure may be formed on the surface of a shield wafer. If such shield wafer is used n-times, a 2n-layered porous layer is formed in the shield wafer. The porous layer becomes extremely unstable. For example, a porous portion formed at the shield wafer has been peeled off at n + 1 times, and sometimes has diffused in a container. In particular, when the lowly and highly porous layers are formed alternately, the mechanical strength is lowered more significantly than a case in which a porous layer having the same thickness is formed under constant forming conditions. That is, use of the shield wafer has been limited. However, according to the present invention, a two or more layered structure of the porous layer of the first substrate is determined depending on a structure of the epitaxially grown layer formed in advance on the surface of the first substrate. Thus, the density of current to be applied to the shield wafer can be made constant, and the service life of the shield wafer can be extended.

[0168] A two or more layers may be provided for the structure of the porous layer. In particular, a highly porous layer may be formed for a second layer from the surface, and a second lowly porous layer may be formed thereunder. In this situation, even if a defect is introduced during separation, such defect in the porous layer can be removed in the subsequent step of removing the porous layer and the defect does not remain in the first substrate. Thus, when three or more layered structure of the porous layer is formed, a layer having its different composition, impurity concentration, and type, suitable to these porous layers, is formed in an epitaxially grown layer.

[0169] Then, in FIG. 8C, a non-porous layer 5 is formed on a porous layer 4, and a first member is formed. A method for forming the non-porous layer 5 includes closing the pores of the porous layer 4 to make the top layer porous by hydrogen annealing or forming a non-porous monocrystalline layer by epitaxial growth. The surface of the non-porous layer 5 is oxidized as required, thereby forming an insulating layer 6 on the non-porous layer 5. Instead of heat oxidizing, the insulating layer 6 may be formed by CVD or sputtering and the like. In this embodiment a porous portion of the epitaxial semiconductor layer 31 is employed as a separation layer.

[0170] In FIG. 8D, the surface of the insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multilayer structure. A second wafer 2 being a second member consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like is provided. The second wafer may be a wafer on which a semiconductor is exposed or may have an insulating film on its surface. Alternatively, an insulating light transmission substrate such as quartz glass may be employed instead of the second wafer. In bonding, these surfaces may be subjected to heat treatment at room temperature in contact with each other to increase bonding strength or may be bonded with each other by anode bonding. Alternatively, the surfaces may be subjected to heat treatment at the same time when they comes into contact with each other. Further, in the bonding step, heat treatment or the like may be carried out while they are pressurized so as to come into closer contact with each other.

[0171] In addition, it is preferable to apply plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least one of a pair of bonding faces, and activate in advance these bonding faces. Further, a bonding layer may be intervened between these surfaces to be bonded.

[0172] In FIG. 8E, at the separation layer (porous portion of the epitaxial semiconductor layer 31), a multilayer structure is separated by the aforementioned method. The non-porous portion of the peeled first wafer is maintained to a wafer shape, and has a remaining portion 41 of the porous layer on the separated face (a part of the porous portion of the epitaxial semiconductor layer 31). On the other hand, on the second wafer 2, the non-porous layer 5 transferred from the first wafer is provided together with the insulating layer 6, and has a remaining portion 42 of the porous layer on its separated face (a part of the porous portion of the epitaxial layer 32 and the porous portion of the epitaxial semiconductor layer 31).

[0173] In FIG. 8F, the remaining portion 42 is removed. When the thickness of the remaining portion 42 is relatively thick, a mixture of fluoric acid, hydrogen peroxide, and alcohol is employed as an etchant, and the remaining portion 42 is removed by selectively conducting wet etching on it, and then, the surface is smoothed by hydrogen annealing. When thickness of the remaining portion 42 is thin, hydrogen annealing may be carried out without wet etching, and smoothing treatment may be carried at the same time when the remaining portion 42 is removed. Thus, a highly value-added SOI wafer is obtained.

[0174] In FIG. 8G, the remaining portion 41 on the wafer 1 (a semiconductor substrate) after peeling is removed by

polishing, wet etching, and hydrogen annealing, and is smoothed.

[0175] At this time, a non-porous layer (epitaxial layer) 10 remains on the wafer 1, and an epitaxial wafer is obtained. When a wafer other than P-type silicon wafer is desired on a substrate beneath as an epitaxial wafer after separation, a desired silicon wafer (for example, P^- or N type) can be employed.

[0176] In these steps, two or more epitaxial semiconductor layers 31 may be formed. For example, when the two epitaxial semiconductor layers are formed, epitaxial semiconductor layers 31' and 31" (31 in all) are formed in this order. The epitaxial semiconductor layers are made porous, which is carried out from the epitaxial semiconductor layer 32 on the surface. Until at least monocrystalline semiconductor layer 31" is made porous, the layers are made porous so that a part of the epitaxial semiconductor layer 31' remains without being made porous. Therefore, when the layer 31' is made porous part-way, the epitaxial semiconductor layer 31', porous layer 41' (a layer obtained by making part of the epitaxial semiconductor layer 31' porous), porous layer 41" (a layer obtained by making the epitaxial semiconductor layer 31" porous), and porous layer 42 (a layer obtained by making the monocrystalline semiconductor layer 32 porous) are formed in that order from the first wafer 1. In addition, when the interface between the monocrystalline semiconductor layer 31" and the monocrystalline semiconductor layer 31' is made porous, the porous layer 41' (a layer obtained by making the single semiconductor layer 31' porous) does not exist.

[Role of each layer]

[0177] Epitaxial layer 32: A good-quality epitaxial layer (SOI) is formed on this porous layer.

[0178] Epitaxial layer 31': A remaining layer without being made porous becomes an epitaxial layer for a second semiconductor substrate.

[0179] Epitaxial layer 31": Separation is conducted inside of the thus formed porous layer or at a upper- or lower-interface thereof

[0180] In FIG. 8G, the remaining portion 41 on the wafer 1 (semiconductor substrate) after peeling is removed by polishing, wet etching, hydrogen annealing or the like, and is smoothed. At this time, the epitaxial layer 10 (original monocrystalline semiconductor layer 31) formed in FIG. 8A remains. When hydrogen annealing is applied in this state, the surface is smoothed. When the concentration of boron contained is higher than a desired concentration, the boron concentration is lowered by outward diffusion, and the layer 10 is formed as a P^- type monocrystalline semiconductor layer.

[0181] This is a wafer of the same quality as a so-called P^- epitaxial wafer. The boron concentration of this layer is substantially equal to that of the initial epitaxial semiconductor layer 31. This layer is made porous in a region close to the surface (porous layer 42), and acts as a separation layer. Thus, there is a possibility that the boron concentration thereof does not match with that for a P^- epitaxial wafer. In this case, as described above, two or more epitaxial semiconductor layers 31 having different boron concentrations are arranged, whereby these layers may be formed by being divided into a layer (31") having its optimum boron concentration to make it porous for separation and a layer (31') having its optimum boron concentration for a P^- epitaxial wafer. If there is no need for positively conducting outward diffusion, even if the surface is smoothed by polishing or short-time hydrogen annealing, a wafer of the same quality as the P^- epitaxial wafer is formed. Thus, one SOI wafer and one epitaxial wafer that are highly value-added are obtained from two wafers. This epitaxial wafer is diverted or is sold as a wafer employed for various uses other than being used for manufacturing an SOI wafer, whereby an economically advantageous SOI wafer manufacturing process can be constructed. Moreover, it is possible to manufacture an SOI wafer using a new wafer all the time, and thus, its production efficiency is increased.

(Embodiment 8)

[0182] FIGS. 9A to 9G are schematic views showing a method for manufacturing a wafer according to an Eighth Embodiment of the present invention.

[0183] First, in FIG. 9A, a first wafer 1 consisting of a P-type silicon wafer is provided, and an epitaxial layer 31 of a first specific resistance of a first conductive type (for example P^-) and an epitaxial layer 32 of a second specific resistance of a second conductive type (for example, 'n') are formed on its surface by epitaxial growth. In this embodiment, an epitaxial layer 32 is formed as an active layer on the SOI wafer, and an epitaxial layer 31 is formed as an active layer on the epitaxial wafer. The respective active layers can be fabricated by epitaxial growth of a series of steps. The epitaxial layers 31 and 32 may be of the same conductive type (P type or N type), and the specific resistance may be the same without being changed in particular (that is, a single epitaxial layer may be formed). The monocrystalline semiconductor layers 31 and 32 are finally formed as an epitaxial wafer and a surface semiconductor layer of a wafer such as SOI, and thus, the conductive type and concentration of impurities are preferably optimized for respective uses. As a first wafer, a high concentration P-type silicon wafer is preferably employed.

[0184] In FIG. 9B, the surface of the epitaxial layer 32 of the first wafer is thermally oxidized etc., thereby forming

an insulating layer 6 (FIG. 9C). Next, an ion selected from hydrogen, nitrogen, or rare gas is implanted, and a layer 14 containing fine cavities being a separation layer at a predetermined depth is formed. The position of the separation layer is specified so that at least a part (non-porous layer 5) of the monocrystalline semiconductor 32 remains on the separation layer 14, and further, at least a part (non-porous layer 10) of the monocrystalline semiconductor 31 remains below the separation 14. Thus, a first member is formed.

[0185] At this time, it is preferable to implant an ion into the epitaxial layer 31 and/or the epitaxial layer 32 so that a non-porous epitaxial layer 10 (a part of the epitaxial layer 31) remains below the separation layer 14 with a thickness of 10 nm to 20 μm. Here, there is shown a case in which a separation layer 14 is formed so that the interface between the epitaxial layers 31 and 32 exists in the separation layer 14 (that is, in such a manner that a separation layer is formed between the epitaxial layers 31 and 32).

[0186] In FIG. 9D, the surface of the insulating layer 6 of the first wafer 1 and the surface of the second wafer 2 are bonded with each other to form a multilayer structure. A second wafer being a second member consisting of a bulk wafer such as a CZ silicon wafer, an FZ silicon wafer or the like may be a wafer on which a semiconductor is exposed or may have an insulating film on its surface. Alternatively, an insulating light transmission substrate such as quartz glass may be employed instead of the first wafer. These surface may be bonded with each other at room temperature. In bonding, the surfaces may be subjected to heat treatment in contact with each other at room temperature to increase bonding strength or may be bonded with each other by anode bonding. Alternatively, heat treatment may be carried out at the same time when these surfaces come into contact with each other. Further, in the bonding step, heat treatment or the like may be carried out while the surfaces are pressurized so as to come into closer contact with each other. In addition, a bonding layer is intervened between these surface to be bonded. In addition, it is preferable to apply plasma treatment using oxygen, nitrogen, silicon, hydrogen, rare gas or the like to at least either one of a pair of bonding faces, and activate the bonding face in advance.

[0187] In FIG. 9E, at the separation layer 14, a multilayer structure is separated by the aforementioned method. In the method of this example, when a temperature is set to 400°C or above and preferably 400°C to 600°C during heat treatment shown in FIG. 9D, a separation phenomenon may occur at the same time as bonding.

[0188] The peeled first wafer 1 is maintained to a wafer shape without a decrease in thickness, and has a remaining portion 141 of the separation layer 14 on the separated face. On the other hand, on the second wafer, a non-porous layer 5 transferred from the first wafer is provided together with an insulating layer 6, and has a remaining portion 142 of the separation layer 14 on its separated face. In FIG. 9F, the remaining portion 142 is removed. The remaining portion 141 is removed by polishing, wet etching, hydrogen annealing or the like, and is smoothed. Thus, a highly value-added SOI wafer is obtained.

[0189] In FIG. 9F, the remaining portion 142 is removed. At this time, the remaining portion may be polished at a low polishing rate, and then, may be subjected to hydrogen-annealing. Alternatively, hydrogen annealing may be carried out without polishing, and smoothing treatment may be carried out at the same time when the remaining portion 142 is removed. Thus, a highly value-added SOI wafer is obtained.

[0190] In FIG. 9G, the remaining portion 141 on the wafer 1 (semiconductor substrate) after peeling is removed by polishing, wet etching, hydrogen annealing or the like, and is smoothed. At this time, the epitaxial layer 10 formed in FIG. 9A remains. When hydrogen annealing is applied in this state, the surface is smoothed, and the concentration of boron contained is lowered by outward diffusion, thereby making it possible to employ the layer 10 as a P^- type monocrystalline semiconductor layer. Thus, one SOI wafer and one epitaxial wafer (for example, a wafer on which a P^- epitaxial layer is formed on a P^+ substrate) can be obtained from two wafers.

[0191] Hereinafter, a manufacturing system (a manufacturing plant) suitable to implement the manufacturing methods of the above embodiments 7 and 8 will be described.

[0192] FIG. 13 is a schematic view illustrating an example of the manufacturing system. The manufacturing system of FIG. 13 is merely different from a part of the manufacturing system of FIGS. 6A to 6G, and thus elements identical to those of FIGS. 6A to 6G are designated by the same reference numerals, a description there of will be omitted here.

[0193] The manufacturing system of FIG. 13 is different from that of FIGS. 6A to 6G in that an epitaxial layer is formed on a first substrate (wafer) 1, and then, is sent to a group of processing apparatuses 51 having an anodization apparatus, an epitaxial growth apparatus, an ion implanting apparatus, an oxidizing apparatus or the like, i.e., when the peeled first substrate is smoothed at a group of apparatuses 54, the epitaxial wafer 21 is completed (that is, there is no need for performing new epitaxial growth to form an epitaxial layer).

(Manufacturing System)

[0194] Hereinafter, a manufacturing system (a manufacturing plant) suitable to implement a wafer manufacturing method of the present invention will be described.

[0195] FIG. 10 is a schematic view illustrating an example of the manufacturing system. As shown in the figure, a first substrate (wafer) 1 is sent to a group of processing apparatuses 51 having an anodization apparatus, an epitaxial

growth apparatus,- an ion implanting apparatus, an oxidizing apparatus or the like, and the aforementioned step S2 or the like is implemented.

[0196] The first substrate 1 having a separation layer formed thereon is sent to a group of bonding apparatuses 52, and is bonded with a second substrate (wafer) 2 therein, and a multilayer structure is obtained.

[0197] The multilayer structure is sent to a group of separation apparatuses 53 containing at least a water jet apparatus, a teat treatment apparatus, a wedge inserting apparatus or the like, and is separated therein.

[0198] The second substrate after peeling is sent to a group of separation-layer-removing and surface-smoothing apparatuses 54 containing an etching apparatus, a polishing apparatus, a heat treatment apparatus or the like. Then, the substrate is subjected to treatment, and an SOI wafer 20 is completed.

[0199] On the other hand, the peeled first substrate is smoothed in a group of apparatuses 54 and is completed as a bulk wafer, or is sent to an epitaxial growth apparatus 55. Then, epitaxial growth treatment is applied, and an epitaxial wafer 21 is completed.' Of course, in the processing apparatuses 51, when epitaxial growth is conducted on the first substrate 1, an epitaxial wafer is obtained at the same time as when it is separated, thus making it possible to disuse the epitaxial growth apparatus 55.

[0200] These SOI wafer 20 and epitaxial wafer 21 (or bulk wafer) are sent to a group of inspection and analysis apparatuses 56; film thickness distribution, foreign particle density, and defect density or the like are measured; and the wafer is packed in a group of shipment packing apparatuses 57, and is then shipped. The epitaxial wafer 21 is diverted or sold as a wafer for other various uses other than being used as a first substrate 1 or a second substrate 2. Reference numeral 58 designates a maintenance area; and reference numeral 59 designates a clean area for conveying a wafer. Thus, two wafers are employed, and one SOI wafer and one epitaxial wafer (or bulk wafer) can be fabricated. A new wafer can always be employed for manufacture of SOI wafers. An efficient semiconductor manufacturing process can be constructed by diverting a wafer for another uses and selling the wafer that has been conventionally re-utilized in the same process or discarded.

[0201] FIG. 11 is a view showing a partial modification of a system of FIG. 10, wherein the obtained SOI wafer 20 and epitaxial wafer 21 (or a bulk wafer) are separately inspected so as to be packed.

[0202] In this case, when the epitaxial wafer 21 is required to have the same quality as the obtained SOI wafer 20, the epitaxial wafer 21 (or a bulk wafer) is not used as a first substrate 1 or a second substrate 2 again. Thus, one SOI wafer and one epitaxial wafer can be manufactured from two wafers, and a manufacturing process with its efficient wafer utility can be constructed.

[0203] FIG. 12 is a flowchart of the inspection step for determining use to which a first wafer after peeling is diverted.

[0204] As shown in FIG. 12, a foreign matter on the surface of the wafer after peeling is first measured (step S50). When a surface foreign matter is not measured or is below a standard value, surface roughness is then measured based on a first standard (low standard) (step S51). When the first standard of the surface roughness is met, the surface roughness is measured based on a second standard (a standard higher than the first standard) (step S52). When the second standard of the surface roughness is met, edge portion judgment is performed (step S53). If there is no problem with an edge portion, the first wafer is produced, and is employed as an apparatus wafer, an epitaxial wafer, or a high-quality dummy wafer (step S54).

[0205] When the surface foreign matter exceeds the standard value in step S50 or when surface roughness does not meet the first standard in step S51, surface re-treatment such as re-washing, re-polishing or the like is performed (step S55). After the surface re-treatment, the wafer is inspected again in the steps S50 to S54 or is employed as a dummy wafer if required (step S56). In addition, if the surface roughness does not meet the second standard in step S52, the wafer is employed as a dummy wafer (step S56).

[0206] If there is a problem with edge judgment in step S53, edge re-treatment such as edge polishing is performed (step S57). The wafer in which no specification for edge is required is produced as it is, and is employed as an apparatus wafer, a epitaxial wafer, or a high-quality dummy wafer (step S54).

[0207] Hereinafter, a manufacturing system (a manufacturing plant) suitable to implement the manufacturing methods of the above embodiments 7 and 8 will be described.

[0208] FIG. 13 is a schematic view illustrating an example of the manufacturing system. The manufacturing system of FIG. 13 is partially different from that of FIG. 10, and thus elements identical to those of FIG. 10 are designated by the same reference numerals, and a description thereof is omitted.

[0209] The manufacturing system of FIG. 13 is different from that of FIG. 10 in that an epitaxial layer is formed on a first substrate (wafer) 1, and then, is sent to a group of processing apparatuses 51 having an anodization apparatus, an epitaxial growth apparatus, an ion implanting apparatus, an oxidizing apparatus or the like; i.e., when the peeled first substrate is smoothed in a group of apparatuses 54, an epitaxial wafer 21 is completed (that is, there is no need for perform new epitaxial growth to form an epitaxial layer).

[0210] FIG. 14 is a view showing a partial modification of the system of the FIG. 13, wherein the obtained SOI wafer 20 and the epitaxial wafer 21 (or a bulk wafer) are separately inspected, and packed. The manufacturing system of FIG. 14 is partially different from that of FIG. 11. The manufacturing system of FIG. 14 is different from that of FIG. 11

in that an epitaxial layer is formed on the first substrate (wafer) 1, and then, is sent to a group of processing apparatuses 51 having an anodization apparatus, and an epitaxial growth apparatus, an ion implanting apparatus, and an oxidizing apparatus or the like; i.e., when the peeled first substrate is smoothed in a group of apparatuses 54, the epitaxial wafer 21 is completed (that is, there is no need for performing epitaxial growth to form an epitaxial layer.

[0211] The inspection step for determining use to'which a first wafer after peeling is diverted is the same as the flowchart shown in FIG. 12.

[0212] Now, the present invention will be described by way of examples.

[0213] In the following examples, it is noted that 80 Torr is equivalent to about 1.07×10^4 Pa expressed in the SI unit system. Similarly, 760 Torr is equivalent to about 1.01×10^5 Pa, 0.5 l/min. is equivalent to about 0.0083 L/S, 180 l/min. is equivalent to 3 L/S, and 0.2 l/min. is equivalent to about 0.0033 L/S.

(Example 1)

[0214] A first p-type monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 Ω-cm was anodized in an HF solution.

[0215] The conditions of the anodization are listed below.

current density	7 ($mA\text{-}cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	11 (minutes)
thickness of porous Si	12 (μm)

[0216] The porous Si was also used as a separation layer for forming a high quality epitaxial Si layer. Therefore, it was a multi-functional layer. Note that the thickness of the porous Si layer may have a value selected from a range between 0.1 and 600 μm.

[0217] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the inner walls of the pores of the porous Si layer were covered by thermally oxidized film. Then, monocrystalline Si was made to epitaxially grow to a thickness of 0.3 μm. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.15 μm / min.

[0218] Then, a 100nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0219] Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment to produce a multilayer structure.

[0220] A wedge of a rigid material was driven into the multilayer structure from a lateral side thereof to peel the multilayer structure and remove the first substrate from the multilayer structure. As a result of the peeling, the epitaxial layer was transferred onto the second substrate.

[0221] The porous layer remaining on the epitaxial layer was removed by wet etching and the second substrate was subjected to a hydrogen annealing process to obtain an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0222] On the other hand, the exposed surface of the peeled first substrate was polished to remove the residual porous layer and smoothed to obtain a bulk wafer, which was then used to prepare a CMOS logic circuit.

[0223] It was also possible to prepare a solar cell by using the obtained bulk wafer in a manner as described below.

[0224] Firstly, after forming a porous layer 4 by anodization, an epitaxial layer 5 was made to grow as shown in FIG. 16A.

[0225] More specifically, the epitaxial growth of the semiconductor film 5 was conducted in a manner as described below. A first semiconductor layer 503 of p^+ Si was formed by epitaxial growth in an atmospheric pressure Si epitaxial growth system, using SiH_4 gas and B_2H_6 gas to dope the p^+ Si of the first semiconductor layer 503 with boron B for 3 minutes to obtain a boron concentration of 10^{19} atoms/cm^3. Then, a second semiconductor layer 502 was formed in

the same system by altering the B_2H_6 gas flow rate to dope the p^- Si of the second semiconductor layer 502 with boron B for 10 minutes to get a low boron concentration of 10^{16} atoms/cm^3. Thereafter, a third semiconductor layer 501 was formed on the p^- epitaxial semiconductor layer 502 also by epitaxial growth using PH_3 gas in place of B_2H_6 gas to dope the n^+ Si of the third semiconductor layer 501 with phosphor for 4 minutes to get a high phosphor concentration of 10^{19} atoms/cm^3. Thus, the obtained semiconductor film 5 of the first through third epitaxial semiconductor layers 501 through 503 showed a $p^+ / p^- / n^+$ structure.

[0226] Then, in this example, a transparent SiO_2 insulating film 80 was formed on the semiconductor film 5 by surface thermal oxidation and subjected to a pattern etching operation using a photolithography technique to make it contact with electrodes or wires 81. The wires 81 were arranged with required intervals to extend in parallel with each other as so many stripes in a direction perpendicular to the drawing.

[0227] Each of the electrodes or the wires 81 was made of a metal film prepared as multilayer film by sequentially depositing Ti film, a Pd film and an Ag to respective thicknesses of 30nm, 50nm and 100nm by evaporation and thereafter plating the surface with Ag. The obtained multilayer film was then annealed at 400 °C for 20 to 30 minutes.

[0228] Then, a metal wire conductor 82 was bonded to the surface of each of the stripe-shaped electrodes or the wires 81 to extend along the corresponding wire 81 and a transparent substrate 83 was bonded onto the conductors 82. The conductors 82 may be bonded to the electrodes or the wires 81 by soldering. The conductors 82 were extended externally at an end thereof beyond the electrodes or the wires 81.

[0229] Thereafter, the bulk wafer 1 and the transparent substrate 83 were subjected to external force trying to separate them from each other. Then, they were separated along the porous layer 4 to produce a thin film semiconductor 86 comprising a transparent substrate 83 and an epitaxial semiconductor film 5 bonded onto the surface of the substrate 83.

[0230] While the porous layer 41 was partly left on the rear surface of the thin film semiconductor 86, silver paste was applied thereon and a metal plate was bonded thereto to produce a rear surface electrode 85 there. Thus, a solar cell comprising a transparent substrate 83 and a thin film semiconductor 86 having a $p^+ / p^- / n^+$ structure was prepared (FIG. 16C). The metal electrode 85 operates also as a device protection film layer protecting the rear surface of the solar cell.

[0231] Note that the porous layer 4 may be made to have a multilayer structure of layers with different porosities as shown in FIG. 16D.

[0232] For instance, the layer 401 may have a low porosity (to produce a high quality epitaxial film) and the layers 402 and 404 may be made to show a porosity higher than that of the layer 401, while the layer 403 may be made to show the highest porosity of all.

[0233] With such an arrangement, the bulk wafer 1 and the transparent substrate 83 can be separated effectively along the high porosity layer 403. Layers with different porosities can be formed by controlling the current density during the process of forming the porous layer.

(Example 2)

[0234] A first p-type monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 Ω·cm was anodized in an HF solution.

[0235] The conditions of the anodization are listed below.

current density	7 (mA·cm^{-2})
anodizing solution	HF:H_2O:C_2H_5OH = 1: 1: 1
time	5 (minutes)
thickness of porous Si	5.5 (μm)
current density	30 (mA·cm^{-2})
anodizing solution	HF:H_2O:C_2H_5OH = 1: 1: 1
time	10 (seconds)
thickness of porous Si	0.2 (μm)

[0236] Of the two porous Si layers, the upper one prepared by anodization, using a low current density, was used to form a high quality epitaxial Si layer, whereas the lower one prepared by anodization, using a high current density, was used as a separation layer. Therefore, they have their respective functions.

[0237] Note that the thickness of the low current density porous Si layer may have a value selected from a range between 0.1 and 600 μm. Also note that one or more than one additional layers may be formed after forming the second porous Si layer.

[0238] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the

inner walls of the pores of the porous Si layers were covered by thermally oxidized film. Then, monocrystalline Si was made to epitaxially grow to a thickness of 0.3 μm by means of CVD. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.3 μm / min.

[0239] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0240] Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment to produce a multilayer structure.

[0241] Water was blown onto a lateral side of the multilayer structure under high pressure by means of a water jet apparatus to make it driven into the multilayer structure like a wedge to peel the multilayer structure and remove the first substrate from the multilayer structure.

[0242] As a result of the peeling, the epitaxial layer was transferred onto the second substrate.

[0243] The porous layer remaining on the epitaxial layer was removed by wet etching and the second substrate was subjected to a hydrogen annealing process to obtain an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0244] On the other hand, the exposed surface of the peeled first substrate was polished to remove the residual porous layer and smoothed. Then, the first substrate was subjected to an epitaxial growth process to obtain an epitaxial wafer having a p^- epitaxial layer on the high concentration p-type substrate. It was found that a 600 nm thick oxide film had been formed on the wafer back surface as back shield. When an epitaxial wafer is used for preparing a device, a surface oxide film is formed on the surface opposite to the epitaxial layer and also on the lateral surfaces as a back shield in order prevent impurities from externally diffusing from the wafer.

[0245] However, since a back shield had been formed on the rear surface opposite to the epitaxial layer and also on the lateral surface of the second substrate when the multilayer structure was peeled, the process of forming a back shield could be omitted from the device preparing process of the example. This was because such a back shield was formed on the rear surface and the lateral surfaces of the wafer in the step of oxidizing the surface of the epitaxial layer preceding the bonding step and during the heat treatment of the bonding step. A similar effect of forming a back shield was observed in the remaining examples. Note that the oxide film has a film thickness of 10 nm to 10 μm, preferably 100 nm to 3 μm.

[0246] Thereafter, the epitaxial wafer was used to prepare a CMOS logic circuit.

[0247] A DRAM and other devices were formed on the epitaxial wafer to prove that it was useful for improving the quality, the yield and the reliability of manufacturing devices.

[0248] The operation of epitaxial growth on the porous Si and that of epitaxial growth on the first substrate after the separation process may be conducted by means of the same CVD system to improve the operating efficiency of the CVD system that is costly in any sense of the word.

(Example 3)

[0249] P-type monocrystalline Si showing a specific resistance of 0.015 Ω·cm was formed on a first monocrystalline Si substrate to a thickness of 15 μm by epitaxial growth, using a CVD technique and then anodized from the surface of the substrate in an HF solution.

[0250] The conditions of the anodization are listed below.

current density	7 ($mA \cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	11 (minutes)
thickness of porous Si	12 (μm)
current density	22 ($mA \cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	2 (minutes)

(continued)

thickness of porous Si	3 (μm)

[0251] Of the two porous Si layers, the upper one prepared by anodization, using a low current density, was used to form a high quality epitaxial Si layer, whereas the lower one prepared by anodization, using a high current density, was used as a separation layer. Therefore, they have their respective functions.

[0252] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the inner walls of the pores of the porous Si layers were covered by thermally oxidized film. Then, monocrystalline Si was made to epitaxially grow to a thickness of 0.3 μm by means of CVD. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.3 μm / min.

[0253] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0254] Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment to produce a multilayer structure.

[0255] Water was blown onto a lateral side of the multilayer structure under high pressure by means of a water jet apparatus to make it driven into the multilayer structure like a wedge to peel the multilayer structure and remove the first substrate from the multilayer structure. As a result of the peeling, the epitaxial layer was transferred onto the second substrate.

[0256] The porous layer remaining on the epitaxial layer was removed by wet etching and the second substrate was subjected to a hydrogen annealing process to obtain an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0257] On the other hand, the exposed surface of the separated first substrate was polished to remove the residual porous layer and subjected to hydrogen annealing to obtain a bulk wafer having a flat surface.

[0258] The obtained bulk wafer was then used to prepare a CMOS logic circuit. It may be needless to say that the bulk wafer may be sold at a price lower than the ordinary market price of a bulk wafer without using it to prepare a logic circuit.

(Example 4)

[0259] P-type monocrystalline Si showing a specific resistance of 0.015 Ω·cm was formed on a first monocrystalline Si substrate to a thickness of 16 μm by epitaxial growth, using a CVD technique and then anodized from the surface of the substrate in an HF solution.

[0260] The conditions of the anodization are listed below.

current density	7 (mA·cm^2)
anodizing solution	HF:H_2O:C_2H_5OH = 1: 1: 1
time	11 (minutes)
thickness of porous Si	12 (μm)
current density	22 (mA·cm^{-2})
anodizing solution	HF:H_2O:C_2H_5OH = 1: 1: 1
time	2 (minutes)
thickness of porous Si	3 (μm)

[0261] Of the two porous Si layers, the upper one prepared by anodization, using a low current density, was used to form a high quality epitaxial Si layer, whereas the lower one prepared by anodization, using a high current density, was used as a separation layer. Therefore, they have their respective functions.

[0262] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the

inner walls of the pores of the porous Si layers were covered by thermally oxidized film. Then, monocrystalline Si was made to epitaxially grow to a thickness of 0.3 μm by means of CVD. The conditions of the epitaxial growth are listed below.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.3 μm / min.

[0263] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0264] Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment to produce a multilayer structure.

[0265] Water was blown onto a lateral side of the multilayer structure under high pressure by means of a water jet apparatus to make it driven into the multilayer structure like a wedge to peel the multilayer structure and remove the first substrate from the multilayer structure. As a result of the peeling, the epitaxial layer was transferred onto the second substrate.

[0266] The porous layer remaining on the epitaxial layer was removed by wet etching and the second substrate was subjected to a hydrogen annealing process to obtain an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0267] On the other hand, the exposed surface of the peeled first substrate was polished to remove the residual porous layer and the epitaxial layer that had not been made porous and subjected to hydrogen annealing to externally disperse the residual epitaxial layer and obtain a bulk wafer that performed substantially in the same level as an epitaxial wafer.

[0268] The obtained bulk wafer was then used to prepare a CMOS logic circuit.

(Example 5)

[0269] A 200nm thick SiO_2 layer was formed on the surface of a first monocrystalline Si substrate by thermal oxidation.

[0270] Then, H^+ ions were implanted into the first substrate from the surface thereof at a rate of $5\times10^{16}cm^{-2}$ by applying a voltage of 40 keV so as to confine the projection range within the Si substrate. As a result, a strained layer was formed at the depth corresponding to the projection range as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0271] Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment at 500 °C to produce a multilayer structure, which was then separated into the first substrate and the second substrate.

[0272] As a result of the split, the epitaxial layer was transferred onto the second substrate.

[0273] The residual separation layer on the surface of the monocrystalline semiconductor layer transferred onto the second substrate was removed by hydrogen annealing and the surface was smoothed to produce an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0274] On the other hand, the exposed surface of the separated first substrate was found to be carrying part of the separation layer, which was then removed by hydrogen annealing. Then, the surface was smoothed to produce a bulk wafer. Subsequently, a low concentration p-type epitaxial layer was formed thereon to obtain an epitaxial wafer.

(Example 6)

[0275] Monocrystalline Si was made to epitaxially grow on a first monocrystalline Si substrate to a thickness of 1 μm by means of CVD. The conditions of the epitaxial growth are listed below.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.30 μm / min.

[0276] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0277] Then, H^+ ions were implanted into the first substrate from the surface thereof at a rate of $5\times10^{16}cm^{-2}$ by applying a voltage of 40 keVso as to confine the projection range within the Si substrate. As a result, a strained layer was formed at the depth corresponding to the projection range as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0278] Subsequently, a silicon wafer (second substrate) having the same diameter and carrying an oxide film formed on the surface thereof was treated by nitrogen plasma at the surface to be bonded thereof and then the first and second substrate were brought to contact each other and bonded together to produce a multilayer structure. A water jet was blown onto a lateral side of the multilayer structure and driven toward the center of the multilayer structure to separate it into the first and second substrates.

[0279] As a result of the split, the epitaxial layer was transferred onto the second substrate.

[0280] The residual separation layer on the surface of the epitaxial layer transferred onto the second substrate was removed by hydrogen annealing and the surface was smoothed to produce an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0281] On the other hand, the exposed surface of the separated first substrate was found to be carrying the epitaxial layer and part of the separation layer thereon, which was then removed by hydrogen annealing. Then, the surface was smoothed to obtain a bulk wafer. The bulk wafer had a surface layer produced by hydrogen annealing the epitaxial layer and hence performed substantially in the same level as an epitaxial wafer.

[0282] The obtained bulk wafer was then used to prepare a CMOS logic circuit.

(Example 7)

[0283] A 100nm thick SiO_2 layer was formed on the surface of a first monocrystalline substrate by thermal oxidation.

[0284] Then, H^+ ions were implanted into the first substrate from the surface thereof at a rate of $5\times10^{16}cm^{-2}$ by applying a voltage of 30 keV so as to confine the projection range within the Si substrate. As a result, a strained layer was formed at the depth corresponding to the projection range as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0285] After removing the surface oxide film, amorphous Si or polycrystalline Si was made to grow on the surface of the monocrystalline Si to a thickness of 0.30 μm by means of CVD. The conditions of the growth are listed below.

gas seeds	SiH_4
gas pressure	760 Torr
temperature	400 °C

[0286] Thereafter, a 200nm thick SiO_2 layer was formed on the surface.

[0287] Then, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment at 600 °C to produce a multilayer structure, which was subsequently separated into the first and second substrates.

[0288] As a result of the split, the monocrystalline semiconductor layer formed by epitaxial growth was transferred onto the second substrate. The residual separation layer on the surface of the monocrystalline semiconductor layer transferred onto the second substrate was removed by hydrogen annealing and the surface was smoothed to produce an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0289] On the other hand, the exposed surface of the separated first substrate was found to be carrying part of the separation layer, which was then removed by hydrogen annealing. Then, the surface was smoothed to obtain a bulk wafer. For the purpose of the invention, the residue may be removed entirely or partly prior to the hydrogen annealing by polishing or etching.

[0290] The obtained bulk wafer was then used to prepare a CMOS logic circuit.

(Example 8)

[0291] A first p-type monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 Ω·cm was anodized in an HF solution.

[0292] The conditions of the anodization are listed below.

current density	7 ($mA\cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1

(continued)

time	11 (minutes)
thickness of porous Si	12 (μm)

[0293] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the inner walls of the pores of the porous Si layer were covered by thermally oxidized film.

[0294] Then, ions were implanted into the first substrate from the surface thereof so as to confine the projection range within the porous Si layer (or to the porous Si/substrate interface). As a result, a strained layer was formed at the depth corresponding to the projection range as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0295] Then, monocrystalline Si was made to epitaxially grow to a thickness of 0.3 μm on the porous Si layer by means of CVD. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.3 μm / min.

[0296] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation. Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment to produce a multilayer structure.

[0297] Water was blown onto a lateral side of the multilayer structure under high pressure by means of a water jet apparatus to make it driven into the multilayer structure like a wedge to peel the multilayer structure and remove the first substrate from the multilayer structure. As a result of the peeling, the epitaxial layer was transferred onto the second substrate.

[0298] The porous layer remaining on the epitaxial layer was removed by wet etching and the second substrate was subjected to a hydrogen annealing process to obtain an SOI wafer. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0299] On the other hand, the exposed surface of the peeled first substrate was subjected to an epitaxial growth process to obtain an epitaxial wafer. Note that the residual porous layer may be completely removed before the epitaxial growth process.

[0300] The obtained epitaxial wafer was then used to prepare a CMOS logic circuit.

[0301] A DRAM and other devices were formed on the epitaxial wafer to prove that it was useful for improving the quality, the yield and the reliability of manufacturing devices.

(Example 9)

[0302] A first p-type monocrystalline Si substrate showing a specific resistance of 0.01 Ω·cm was anodized in an HF solution.

[0303] The conditions of the anodization are listed below.

current density	7 ($mA\cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	12 (minutes)
thickness of porous Si	11 (μm)

[0304] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the inner walls of the pores of the porous Si layer were covered by thermally oxidized film. Then, monocrystalline Si was made to epitaxially grow to a thickness of 0.3 μm on the porous Si layer by means of CVD. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.3 μm / min.

[0305] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0306] Then, ions were implanted into the first substrate from the surface thereof so as to confine the projection range to the epitaxial layer/porous Si layer interface (or the porous Si/substrate interface or within the porous Si layer). As a result, a strained layer was formed at the depth corresponding to the projection range as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0307] Thereafter, a silicon wafer having the same diameter from the surface of which the native oxide film had been removed was brought into contact with the silicon wafer and bonded together by heat treatment at 1,000 °C to produce a multilayer structure, which was then separated. As a result of the separation, the epitaxial layer was transferred onto the second substrate.

[0308] Since practically no porous layer was remaining on the epitaxial layer, the second substrate was subjected to a hydrogen annealing process to obtain an SOI wafer without wet etching. Then, a fully depletion type thin film transistor was prepared by using the SOI wafer.

[0309] On the other hand, the exposed surface of the separated first substrate was polished to obtain a bulk wafer.

[0310] The obtained bulk wafer was then used to prepare a CMOS logic circuit.

[0311] In stead of bonding the second substrate of any of the above examples, polycrystalline silicon may be formed on the uppermost surface of the first substrate to a thickness of 200 to 800 microns by means of a deposition technique such as CVD. Still alternatively, the obtained structure may be split into a plurality of different wafers, which may be used for respective appropriate applications.

(Example 10)

[0312] An epitaxial growth layer was formed to a thickness of 1 μm on the surface of a first p-type monocrystalline Si substrate by means of CVD. During this process, the concentration of diborane added as a dopant was regulated to make it a p^{++} Si layer showing a specific resistance of 0.015 Ω·cm. The thickness of the wafer was 6.34 μm.

[0313] Then, the epitaxial layer was anodized in a mixture solution of HF and ethanol.

[0314] The conditions of the anodization are listed below.

current density	7 ($mA \cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	12 (minutes)

[0315] It was proved by observing a cross section of a specimen of the anodization product through a high resolution scanning electron microscope that a 10 μm thick porous layer had been formed with a porosity of 20%.

[0316] The wafer was then treated at 400 °C for an hour in an oxygen atmosphere and immersed into a 1.25% aqueous solution of HF for 30 seconds to remove the very thin silicon oxide film on the surface. Then, the wafer was put into an epitaxial growth apparatus to produce a 0.3 μm thick monocrystalline Si layer by epitaxial growth, using a CVD (chemical vapor deposition) technique. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.2/ 180 l /min.
gas pressure	760 Torr
temperature	1,060 °C
growth rate	0.15 μm / min.

[0317] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0318] The wafer was then placed on another Si substrate (support substrate) with the surface of the SiO_2 layer facing the surface of the support substrate and they were brought into mutual contact. Thereafter, they are annealed

at 1,180 °C for 5 minutes to find that they were firmly bonded to each other.

[0319] The bonded wafers were forcibly separated along the highly porous layer. Various techniques may be used to separate them apart including application of pressure, application of tensile or shearing force, application of external pressure by means of a wedge, application of ultrasonic waves, application of heat, generating internal pressure within the porous Si layer by causing it to expand through oxidation, application of a pulse of heat to generate thermal stress in the inside and softening. As a matter of fact it was possible to separate them by any of the above listed techniques. Subsequently, the support substrate was immersed into an aqueous solution of a mixture of HF and hydrogen peroxide to find that the residual porous silicon layer was removed from the surface in about 60 minutes to produce an SOI wafer.

[0320] Then, the obtained wafer was heat treated at 1,100 °C for 4 hours in a hydrogen atmosphere.

[0321] The surface roughness was observed through an atomic force microscope to find that the root means square roughness was 0.2nm within an area of 50 pm square, which was substantially equal to the root mean square roughness of commercially available Si wafers. The specimen was also observed for the crystal defect density to find that the multilayer defect density was 50 defects/cm^{-2}. In other words, a low defect density monocrystalline Si layer was formed on the silicon oxide film layer.

[0322] A similar result was obtained when an oxide film was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on the surfaces of both of them.

[0323] The residual porous layer on the first substrate was immersed into an aqueous solution of a mixture of HF and hydrogen peroxide to find that it was removed in about 30 minutes. The 1 μm thick epitaxial layer on the first p-type monocrystalline Si substrate was then subjected to hydrogen annealing to reduce the impurity concentration. Then, the substrate was used to prepare a CMOS logic circuit.

[0324] A DRAM and other devices were formed on the epitaxial wafer to prove that it was useful for improving the quality, the yield and the reliability of manufacturing devices.

(Example 11)

[0325] An epitaxial growth layer was formed to a thickness of 3 pm on the surface of a first p-type monocrystalline Si substrate by means of CVD. During this process, the concentration of diborane added as a dopant was made to vary in order to produce a 2 μm thick upper surface p^{++} Si layer showing a specific resistance of 0.015 Ω·cm and a 1 μm thick lower surface p^{+} Si layer showing a specific resistance of 0.5 Ω·cm.

[0326] During the epitaxial growth, a source gas of SiH_2Cl_2 / H_2 was supplied at a temperature of 1,110 °C under a pressure of 760Torr, while letting a dopant of 1% B_2H_6 flow at 60 sccm for the P^{++} Si layer and at 0.1 sccm for the P^{+} Si layer at a growth rate of 3.33 μm/min for the epitaxial layer.

[0327] Then, the epitaxial layer was anodized in a mixture solution of HF and ethanol.

[0328] The conditions of the anodization are listed below.

current density	7 ($mA·cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	4 (minutes)

[0329] It was proved by observing a cross section of a specimen of the anodization product through a high resolution scanning electron microscope that a low porosity layer of a porosity of 20% and a high porosity layer of a porosity of 50% had been formed respectively in the 2 μm thick upper surface and the 0.5 μm thick lower surface layer of P^{+} Si layer. The thin high porosity layer was obviously structurally very fragile.

[0330] The wafer was then treated at 400 °C for an hour in an oxygen atmosphere and immersed into a 1.25% aqueous solution of HF for 30 seconds to remove the very thin silicon oxide film on the surface. Then, the wafer was put into an epitaxial growth apparatus to produce a 0.3 μm thick monocrystalline Si layer by epitaxial growth, using a CVD (chemical vapor deposition) technique. The conditions of the epitaxial growth are listed below. Note that the above described hydrogen baking process, the process of supplying a small amount of raw material and the high temperature baking process may be conducted prior to the process of growing monocrystalline Si.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.2/ 180 l /min.
gas pressure	760 Torr
temperature	1,060 °C
growth rate	0.15 μm / min.

[0331] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0332] The wafer was then placed on another Si substrate (support substrate) with the surface of the SiO_2 layer facing the surface of the support substrate and they were brought into mutual contact. Thereafter, they are annealed at 1,180 °C for 5 minutes to find that they were firmly bonded to each other.

[0333] The bonded wafers were forcibly separated along the highly porous layer. Various techniques may be used to separate them apart including application of pressure, application of tensile or shearing force, application of external pressure by means of a wedge, application of ultrasonic waves, application of heat, generating internal pressure within the porous Si layer by causing it to expand through oxidation, application of a pulse of heat to generate thermal stress in the inside and softening. As a matter of fact it was possible to separate them by any of the above listed techniques.

[0334] Subsequently, the support substrate was immersed into an aqueous solution of a mixture of HF and hydrogen peroxide to find that the residual porous silicon layer was removed from the surface in about 60 minutes to produce an SOI wafer.

[0335] Then, the obtained wafer was heat treated at 1,100 °C for 4 hours in a hydrogen atmosphere. The surface roughness was observed through an atomic force microscope to find that the root means square roughness was 0.2nm within an area of 50 μm square, which was substantially equal to the root mean square roughness of commercially available Si wafers. The specimen was also observed for the crystal defect density to find that the multilayer defect density was 50 defects/cm^2.

[0336] In other words, a low defect density monocrystalline Si layer was formed on the silicon oxide film layer.

[0337] A similar result was obtained when an oxide film was formed not on the surface of the epitaxial layer but on the surface of the second substrate or on the surfaces of both of them.

[0338] The residual porous layer on the first substrate was immersed into an aqueous solution of a mixture of HF and hydrogen peroxide to find that it was removed in about 30 minutes. Then, an epitaxial layer was made to grow with a boron concentration lower than that of the first p-type monocrystalline Si substrate in order to produce an epi-wafer. The epi-wafer was used to prepare a CMOS logic circuit.

[0339] A DRAM and other devices were formed on the epitaxial wafer to prove that it was useful for improving the quality, the yield and the reliability of manufacturing devices.

(Example 12)

[0340] Monocrystalline Si was made to epitaxially grow on a first monocrystalline Si substrate to a thickness of 1 μm by means of CVD. The conditions of the epitaxial growth are listed below.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.30 μm / min.

[0341] More specifically, the initial 0.5 microns of the height was a P^- layer of 1 Ω-cm formed by using B_2H_6 as a dopant, while the upper 0.5 microns of the height was a N^- layer of 1 Ω-cm formed by using PH_3 as a dopant.

[0342] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0343] Then, H^+ ions were implanted into the first substrate from the surface thereof at a rate of $5\times10^{16}cm^{-2}$ by applying a voltage of 70 keV so as to confine the projection range within the epitaxial layer. As a result, a strained layer was formed at the depth corresponding to the projection range which was close to the P^-/N^- interface as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0344] Subsequently, a silicon wafer (second substrate) having the same diameter was treated by nitrogen plasma at the surface to be bonded thereof and then the first and second substrate were brought to contact each other and bonded together to produce a multilayer structure, which may or may not be heat treated at about 200 °C.

[0345] A water jet was blown onto a lateral side of the multilayer structure and driven toward the center of the multilayer structure to separate it into the first and second substrates.

[0346] The two substrates could also be separated by heat treatment at 500 °C or by utilizing the effect of crystal rearrangement or that of pressure within microbubbles.

[0347] As a result, the N^- monocrystalline semiconductor layer was transferred onto the second substrate.

[0348] The residual separation layer on the epitaxial layer that had been transferred onto the second substrate was removed by hydrogen annealing and the surface of the epitaxial layer was smoothed to obtain an SOI wafer. A similar SOI wafer could be prepared by touch polishing of the surface in place of hydrogen annealing. Then, the wafer was

used to prepare a fully depletion type thin film transistor.

[0349] On the other hand, the separated first substrate carried the P^- epitaxial layer and a residue of the separation layer on the surface thereof, which was then removed by hydrogen annealing. Then, the surface of the substrate was smoothed to obtain an epi-wafer. A similar epi-wafer could be prepared by touch polishing of the surface in place of hydrogen annealing. Since the bulk wafer had a layer formed by hydrogen annealing of the epitaxial layer on the surface, it performed like an epitaxial wafer. An epi-wafer that is currently most popular as P^- epitaxial/P^+ wafer was obtained by using a P^+ substrate for the first Si wafer. The epi-wafer was then used to prepare a CMOS logic circuit.

[0350] A DRAM and other devices were formed on the epitaxial wafer to prove that it was useful for improving the quality, the yield and the reliability of manufacturing devices.

(Example 13)

[0351] P^- monocrystalline Si was formed to a thickness of 1 μm by epitaxial growth by means of CVD to make it show a specific resistance of about 18 Ω-cm on a first P^+ monocrystalline Si substrate showing a specific resistance between 0.01 and 0.02 Ω-cm.

[0352] The conditions of the epitaxial growth are listed below.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.30 μm / min.

[0353] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0354] Then, H^+ ions were implanted into the first substrate from the surface thereof at a rate of $5\times10^{16}cm^{-2}$ by applying a voltage of 40 keVso as to confine the projection range within the epitaxial layer. As a result, a strained layer was formed at the depth corresponding to the projection range as a microbubble layer or as a layer where the implanted ion seeds showed a high concentration, which then operated as a separation layer.

[0355] Subsequently, a silicon wafer (second substrate) having the same diameter was treated by nitrogen plasma at the surface to be bonded thereof and then the first and second substrate were brought to contact each other and bonded together to produce a multilayer structure. A water jet was blown onto a lateral side of the multilayer structure and driven toward the center of the multilayer structure to separate it into the first and second substrates. The two substrates could also be separated by heat treatment.

[0356] As a result, the monocrystalline semiconductor layer was transferred onto the second substrate.

[0357] The residual separation layer on the surface of the epitaxial layer that had been transferred onto the second substrate was removed by hydrogen annealing and the surface of the epitaxial layer was smoothed to obtain an SOI wafer. Then, the SOI wafer was used to prepare a fully depletion type thin film transistor. Thus, a P^+ substrate can be used for preparing an SOI wafer by implanting hydrogen ions if an epi-layer is utilized.

[0358] On the other hand, the separated first substrate carried the epitaxial layer and a residue of the separation layer on the surface thereof, which was then removed by hydrogen annealing. Then, the surface of the substrate was smoothed to obtain a bulk wafer. Since the bulk wafer had a layer formed by hydrogen annealing of the epitaxial layer on the surface, it performed like an epitaxial wafer.

[0359] The epi-wafer was then used to prepare a CMOS logic circuit.

(Example 14)

[0360] The surface of a first monocrystalline Si substrate was subjected to an anodization process in an HF solution.

[0361] The conditions of the anodization are listed below.

[0362] The conditions for preparing a first porous layer to be prepared first and used as the uppermost layer:

current density	1 ($mA\cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	0.1 (minutes)
thickness of porous Si	0.02 (μm)

[0363] The conditions for preparing a second porous layer to be prepared next:

current density	50 ($mA \cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	5 (seconds)
thickness of porous Si	0.1 (μm)

[0364] The conditions for preparing a third porous layer to be prepared last:

current density	7 ($mA \cdot cm^{-2}$)
anodizing solution	$HF:H_2O:C_2H_5OH$ = 1: 1: 1
time	1 (minutes)
thickness of porous Si	1 (μm)

[0365] As a result of the anodization, the second porous layer that was thicker than the first porous layer and prepared with a current density of 50 ($mA \cdot cm^{-2}$) showed the highest porosity of all the porous Si layers and hence was structurally most fragile.

[0366] The substrate was then oxidized for an hour in an oxygen atmosphere at 400 °C. As a result of oxidation, the inner walls of the pores of the porous Si layer were covered by thermally oxidized film. The wafer was placed in an epitaxial growth apparatus filled with a hydrogen atmosphere and baked at 1,040 °C for 5 minutes. As a result of the heat treatment (baking), the surface pores of the uppermost porous Si layer were filled. Then, the uppermost surface layer that was the first porous Si layer prepared with a current density of 1 ($mA \cdot cm^{-2}$) was transformed into a non-porous layer through migration of Si atoms.

[0367] Subsequently, monocrystalline Si was made to epitaxially grow on the porous Si having a non-porous surface to a thickness of 0.3 μm by means of CVD (chemical vapor deposition). The conditions of the epitaxial growth are listed below.

source gas	SiH_2Cl_2 / H_2
gas flow rate	0.5 / 180 l /min.
gas pressure	80 Torr
temperature	950 °C
growth rate	0.30 μm / min.

[0368] Then, a 200nm thick SiO_2 layer was formed on the surface of the epitaxial Si layer by thermal oxidation.

[0369] Subsequently, another silicon substrate (second substrate) was brought in and then the first and second substrate were brought to contact each other and heat-treated at 1,180 °C for 5 minutes to find that they were firmly bonded together.

[0370] Then, external force was applied to the bonded substrates. As a result, the second porous layer showing the highest porosity was destroyed and the two substrates were separated along the interface of the non-porous layer and the adjacent porous layer.

[0371] Thus, a 0.2 μm thick monocrystalline Si layer was formed on the Si oxide film of the second substrate to produce an SOI substrate. No porous Si was found remaining on the surface of the monocrystalline Si layer (separation layer). By separating the two substrates along the interface of the non-porous layer and the adjacent porous layer, it is now possible to omit various steps that are normally required to obtain an SOI layer having a smooth surface.

[0372] More specifically, the two substrates could be separated apart along the interface because stress can be intensively generated at and near the interface. This technique of intensively generating stress along an interface can also be used for a hetero-epitaxial film such as SiGe on silicon.

[0373] The porous Si remaining on the first substrate was selectively etched out by immersing it into an aqueous solution of a mixture of 49% hydrofluoric acid and 30% hydrogen peroxide to produce a bulk wafer having a smooth surface. It was used as a device forming wafer or a monitor wafer without being used as first or second substrate as described above.

[0374] As discussed above in detail, the present invention provides a method of manufacturing high quality semiconductor wafers on a mass production basis with an enhanced degree of reproducibility. A method of manufacturing semiconductor wafers according to the invention can provide high quality SOI wafers that can be efficiently used and reused without affecting the supply of wafers to the market.

Claims

1. A process for manufacturing a semiconductor wafer, comprising the steps of:

preparing a first member which has a semiconductor layer on a semiconductor substrate;
transferring said semiconductor layer onto a second member via separating said semiconductor layer from said first member; and
smoothing the surface of said semiconductor substrate after said transferring step so as to use said semiconductor substrate as a semiconductor wafer for purposes other than forming said first and second members.

2. A process for manufacturing a semiconductor wafer, comprising the steps of:

preparing a first member which has a semiconductor layer on a semiconductor substrate with a separation layer arranged therebetween;
transferring said semiconductor layer onto a second member via separating said semiconductor layer through said separation layer; and
smoothing the surface of said semiconductor substrate after said transferring step so as to use said semiconductor substrate as a semiconductor wafer for purposes other than forming said first and second members.

3. A process for manufacturing a semiconductor wafer, comprising the steps of:

preparing a first member which has a semiconductor layer on a p-type semiconductor substrate;
separating said semiconductor layer from said first member to transfer the semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate from which said semiconductor layer has been separated, said low concentration p-type semiconductor layer having an impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

4. A process for manufacturing a semiconductor wafer, comprising the steps of:

preparing a first member which has a semiconductor layer on a p-type semiconductor substrate with a separation layer arranged therebetween;
separating said semiconductor layer through said separation layer to transfer the semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate which has been separated through said separation layer, said low concentration p-type semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

5. A process for manufacturing a semiconductor wafer, comprising the steps of:

forming a separation layer within a p-type semiconductor substrate to form a first member which has a semiconductor layer on said separation layer;
separating said semiconductor layer through said separation layer to transfer the semiconductor layer onto a second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate which has been separated through said separation layer, said low concentration p-type semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

6. A process for manufacturing a semiconductor wafer, comprising the steps of:

preparing a first member which has a semiconductor layer on a p-type semiconductor substrate with a separation layer arranged therebetween;
bonding said first member with a second member to form a multilayer structure;
conducting heat-treatment of said multilayer structure under an oxidizing atmosphere
separating said multilayer structure through said separation layer to transfer said semiconductor layer onto a

second member, thereby forming a first semiconductor wafer; and
conducting epitaxial growth of a low concentration p-type semiconductor layer on said p-type semiconductor substrate which has been separated through said separation layer, said low concentration p-type semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of said p-type semiconductor substrate.

7. A process for manufacturing a semiconductor wafer, comprising the steps of:

preparing a first member which has at least a first semiconductor layer comprising an epitaxial semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of a p-type semiconductor substrate; a separation layer; and a second semiconductor layer; arranged on said p-type semiconductor substrate in the order as mentioned; and
forming a first semiconductor wafer via transferring said second semiconductor layer onto a second member through the separation step of separating said second semiconductor layer through said separation layer, and forming a second semiconductor wafer having said first semiconductor layer on said p-type semiconductor substrate.

8. A process for manufacturing a semiconductor wafer, comprising the steps of:

forming at least a first semiconductor layer comprising an epitaxial semiconductor layer having impurity concentration, which defines p-type conductivity, lower than that of a p-type semiconductor substrate; and a second semiconductor layer comprising an epitaxial semiconductor layer having impurity concentration, which defines p-type conductivity, higher than that of said first semiconductor layer; arranged on said p-type semiconductor substrate in the order as mentioned; making said second semiconductor layer and part of said first semiconductor layer porous; and forming a third semiconductor layer onto said second semiconductor layer made porous; thereby forming a first member; and
transferring said third semiconductor layer onto said second member to form a first semiconductor wafer, and forming a second semiconductor wafer comprising said p-type semiconductor substrate having said first semiconductor layer.

9. A process for manufacturing a semiconductor wafer as defined in any one of claims 1 to 8, wherein said semiconductor substrate, said p-type semiconductor substrate, and said p-type silicon substrate are each selected from the group consisting of a CZ silicon wafer, an FZ silicon wafer, an epitaxial silicon wafer, and a hydrogen-annealed silicon wafer.

10. A process for manufacturing a semiconductor wafer as defined in any one of claims 1 to 6, wherein said semiconductor layer is selected from the group consisting of a monocrystalline semiconductor layer, a polycrystalline semiconductor layer, and an amorphous semiconductor layer.

11. A process for manufacturing a semiconductor wafer as defined in any one of claims 2, 4, 5, 6, and 7, wherein said separation layer is selected from the group consisting of a porous layer and a microbubble layer.

12. A process for manufacturing a semiconductor wafer as defined in claim 8, wherein said separation layer and said layer made porous is each formed by anodization treatment.

13. A process for manufacturing a semiconductor wafer as defined in claim 11, wherein said separation layer is formed by ion implantation using a gas selected from the group consisting of hydrogen, nitrogen, and rare gas.

14. A process for manufacturing a semiconductor wafer as defined in claim 13, wherein said ion implantation is plasma immersion ion implantation.

15. A process for manufacturing a semiconductor wafer as defined in any one of claims 2, 4, 5, 6, and 7, wherein said first member is obtained by forming a porous layer serving as said separation layer on the surface of said semiconductor substrate followed by forming said semiconductor layer on the surface of said porous layer.

16. A process for manufacturing a semiconductor wafer as defined in claim 15, comprising the additional step of forming a protection layer on the walls of the pores in said porous layer prior to the formation of said semiconductor layer.

17. A process for manufacturing a semiconductor wafer as defined in claim 15, comprising the additional step of conducting heat-treatment on said porous layer under a reducing atmosphere containing hydrogen prior to the formation of said semiconductor layer.

18. A process for manufacturing a semiconductor wafer as defined in claim 15, comprising the step of forming said semiconductor layer by supplying a small amount of raw material gas for said semiconductor layer at a growth rate of 20 mm/min. or lower.

19. A process for manufacturing a semiconductor wafer as defined in claim 15, comprising the additional step of sealing the surface said porous layer followed by conducting heat-treatment at a temperature higher than that for said sealing step prior to the formation of said semiconductor layer, said sealing step comprising the steps of conducting heat-treatment on said porous layer under a hydrogen reducing atmosphere and/or supplying a small amount of raw material gas for said semiconductor layer.

20. A process for manufacturing a semiconductor wafer as defined in any one of claims 2, 4, 5, 6, and 7, wherein said first member is obtained by implanting at least one ion selected from the group consisting of hydrogen, nitrogen, and rare gas into the surface of said semiconductor substrate to form an ion-implanted layer serving as said separation layer within said semiconductor substrate.

21. A process for manufacturing a semiconductor wafer as defined in any one of claims 2, 4, 5, 6, and 7, wherein said first member is obtained by forming an insulating layer followed by forming an ion-implanted layer serving as said separation layer within said semiconductor substrate.

22. A process for manufacturing a semiconductor wafer as defined in claim 1 or 2, wherein said semiconductor substrate comprising said first member is selected from the group consisting of a P^+-silicon wafer and a P^+-silicon wafer.

23. A process for manufacturing a semiconductor wafer as defined in any one of claims 2, 4, 5, 6, and 7, wherein said first member is obtained by the steps of forming an epitaxial layer on said semiconductor substrate, forming said separation layer by making the surface of said epitaxial layer porous, and then forming said semiconductor layer on the surface of said separation layer.

24. A process for manufacturing a semiconductor wafer as defined in claim 23, wherein the surface of said epitaxial layer is made porous such that the thickness of the remaining epitaxial layer on said semiconductor substrate is between 100 nm and 20 μm.

25. A process for manufacturing a semiconductor wafer as defined in claim 23, wherein said epitaxial layer is a P^+ layer in which the concentration of boron is between $1 \times 10^{17} cm^{-3}$ and $1 \times 10^{20} cm^{-3}$.

26. A process for manufacturing a semiconductor wafer as defined in claim 1 or 2, wherein said transferring step comprises the steps of bonding said first member with said second member so as to arrange said semiconductor layer inside to form a multilayer structure and separating said multilayer structure.

27. A process for manufacturing a semiconductor wafer as defined in claim 26, wherein said bonding step is conducted through an insulating layer.

28. A process for manufacturing a semiconductor wafer as defined in claim 26, wherein said bonding step is conducted after forming an insulating layer on the surface of said semiconductor layer.

29. A process for manufacturing a semiconductor wafer as defined in claim 26, wherein said bonding step is conducted after forming an insulating layer on the surface of said second member.

30. A process for manufacturing a semiconductor wafer as defined in claim 26, wherein said separating step is conducted by a method selected from the group consisting of heat-treatment of said multilayer structure and oxidizing treatment of the side of a separation layer and/or the vicinity thereof.

31. A process for manufacturing a semiconductor wafer as defined in claim 30, wherein said heat-treatment is conducted at a temperature within the range of 400 °C to 600 °C

32. A process for manufacturing a semiconductor wafer as defined in claim 26, wherein said separating step is conducted by at least one method selected from the group consisting of inserting a wedge into the side of said separation layer, spraying fluid onto any one of said multilayer structure and the side of said separation layer, applying any one of tensile force, compressive force and shearing force, slicing said multilayer structure at said separation layer, and applying ultrasonic vibration onto said separation layer.

33. A process for manufacturing a semiconductor wafer as defined in claim 32, wherein said fluid is selected from the group consisting of water, alcohols, etchant, air, nitrogen gas, carbonic oxide gas, and rare gas.

34. A process for manufacturing a semiconductor wafer as defined in claim 1 or 2, wherein said semiconductor wafer is an epitaxial wafer.

35. A process for manufacturing a semiconductor wafer as defined in any one of claims 1 to 8, wherein said semiconductor wafer and said second semiconductor wafer are used to manufacture any one of a semiconductor device and a solar battery.

36. A process for manufacturing a semiconductor wafer as defined in any one of claims 1 to 8, wherein said second member is selected from the group consisting of a CZ silicon wafer, a FZ silicon wafer, an epitaxial wafer, a hydrogen-annealed silicon wafer, glass, quartz glass, plastics, a flexible film, ceramic, and a conductive substrate.

37. A process for manufacturing a semiconductor wafer as defined in any one of claims 1 to 8, wherein said second member is a silicon wafer having an oxide film on the surface thereof.

38. A process for manufacturing a semiconductor wafer as defined in claim 1 or 2, wherein said smoothing step is the step of conducting at least one treatment selected from the group consisting of surface-polishing, planing, etching, and heat-treatment.

39. A process for manufacturing a semiconductor wafer as defined in claim 38, wherein said surface-polishing is selected from the group consisting of chemical mechanical polishing and touch-polish.

40. A process for manufacturing a semiconductor wafer as defined in claim 38, wherein said heat-treatment is hydrogen annealing.

41. A process for manufacturing a semiconductor wafer as defined in claim 40, wherein the temperature for said hydrogen annealing is not lower than 800°C and not higher than the melting temperature of the component materials of said semiconductor substrate.

42. A process for manufacturing a semiconductor wafer as defined in claim 40, wherein the hydrogen annealing is a heat-treatment conducted under a reducing atmosphere containing at least hydrogen.

43. A method for using a semiconductor wafer wherein said semiconductor substrate after the smoothing step according to claim 1 or 2 is used as a non-SOI wafer.

44. A method for using a semiconductor wafer wherein said semiconductor substrate after the smoothing step according to claim 1 or 2 is used as a semiconductor wafer to manufacture a semiconductor device.

45. A method for using a semiconductor wafer wherein said semiconductor substrate after the smoothing step according to claim 1 or 2 is used as a dummy wafer.

46. A method for using a semiconductor wafer wherein said semiconductor substrate after the smoothing step according to claim 1 or 2 is used as a monitor wafer.

47. A process for manufacturing a semiconductor wafer as defined in claim 1 or 2, comprising the additional step of forming an epitaxial layer on the smoothed semiconductor substrate.

48. A process for manufacturing a semiconductor wafer as defined in claim 1 or 2, wherein at least one inspection step selected from the group consisting of inspection of the density of surface foreign particles, inspection of film thickness distribution, inspection of the density of defects, inspection of surface profile, and inspection of edges

is conducted on the semiconductor substrate obtained after the smoothing step.

49. A process for manufacturing a semiconductor wafer as defined in claim 48, wherein the substrate is sorted to be used as one wafer selected from the group consisting of a dummy wafer, a monitor wafer, a device wafer, and an epitaxial wafer.

50. A process for manufacturing a semiconductor wafer as defined in any one of claims 3, 4, 5, 7, and 8, wherein said p-type semiconductor substrate is a high concentration p-type silicon wafer.

51. A process for manufacturing a semiconductor wafer as defined in claim 50, wherein the concentration of boron in said high concentration p-type silicon wafer is between $1 \times 10^{17}cm^{-3}$ and $1 \times 10^{20}cm^{-3}$

52. A process for manufacturing a semiconductor wafer as defined in claim 50, wherein the specific resistance of said high concentration p-type silicon wafer is between 0.001 Ω-cm to 0.5 Ω-cm.

53. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 8, wherein the step of forming said first semiconductor wafer comprises the steps of bonding said first member with said second member so as to arrange said semiconductor layer inside to form a multilayer structure and separating said multilayer structure.

54. A process for manufacturing a semiconductor wafer as defined in claim 53, wherein said bonding step is conducted through an insulating layer.

55. A process for manufacturing a semiconductor wafer as defined in claim 53, wherein said bonding step is conducted after forming an insulating layer on the surface of said semiconductor layer.

56. A process for manufacturing a semiconductor wafer as defined in claim 53, wherein said bonding step is conducted after forming an insulating layer on the surface of said second member.

57. A process for manufacturing a semiconductor wafer as defined in claim 53, wherein said separating step is conducted by a method selected from the group consisting of heat-treatment of said multilayer structure and oxidizing treatment of the side of the separation layer and/or the vicinity thereof.

58. A process for manufacturing a semiconductor wafer as defined in claim 57, wherein said heat-treatment is conducted at a temperature within the range of 400 °C to 600 °C

59. A process for manufacturing a semiconductor wafer as defined in claim 53, wherein said separating step is conducted by at least one method selected from the group consisting of inserting a wedge into the side of said separation layer, spraying fluid onto any one of said multilayer structure and the side of said separation layer, applying any one of tensile force, compressive force and shearing force, slicing said multilayer structure at said separation layer, and applying ultrasonic vibration onto said separation layer.

60. A process for manufacturing a semiconductor wafer as defined in claim 59, wherein said fluid is selected from the group consisting of water, alcohols, etchant, air, nitrogen gas, carbonic oxide gas, and rare gas.

61. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 6, wherein the specific resistance of said low concentration p-type silicon layer is between 0.02 Ω-cm to 10000 Ω-cm.

62. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 6, wherein said low concentration p-type silicon layer is an epitaxial silicon layer in which the concentration of boron is $1 \times 10^{17}cm^{-3}$.

63. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 8, wherein at least one inspection step selected from the group consisting of inspection of the density of surface foreign particles, inspection of film thickness distribution, inspection of the density of defects, inspection of surface profile, and inspection of edges is conducted on said second semiconductor wafer.

64. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 6, wherein said epitaxial growth is conducted by a Chemical Vapor Deposition (CVD) method.

65. A process for manufacturing a semiconductor wafer as defined in claim 6, wherein said p-type semiconductor substrate is a high concentration p-type silicon wafer.

66. A process for manufacturing a semiconductor wafer as defined in claim 65, wherein the concentration of boron in said high concentration p-type silicon wafer is between $1 \times 10^{17}cm^{-3}$ and $1 \times 10^{20}cm^{-3}$

67. A process for manufacturing a semiconductor wafer as defined in claim 65, wherein the specific resistance of said high concentration p-type silicon wafer is between 0.001 Ω-cm to 0.5 Ω-cm.

68. A process for manufacturing a semiconductor wafer as defined in claim 7 or 8, wherein said first semiconductor layer is a P^--epitaxial silicon layer.

69. A process for manufacturing a semiconductor wafer as defined in claim 7 or 8, wherein said first semiconductor layer is composed of a plurality of layers.

70. A process for manufacturing a semiconductor wafer as defined in claim 7, wherein said second semiconductor layer has an impurity concentration, which defines p-type conductivity, higher than that of said first semiconductor layer.

71. A process for manufacturing a semiconductor wafer as defined in claim 7, wherein the impurity concentration, which defines p-type conductivity, of said first semiconductor layer is identical with that of said second semiconductor layer.

72. A process for manufacturing a semiconductor wafer as defined in claim 7, wherein said second semiconductor layer and separation layer are formed by ion implantation using a gas selected from the group consisting of hydrogen, nitrogen, and rare gas.

73. A process for manufacturing a semiconductor wafer as defined in claim 8, wherein said third semiconductor layer is an epitaxial monocrystalline silicon layer.

74. A process for manufacturing a semiconductor wafer as defined in claim 7, wherein said first member is obtained by forming said separation layer followed by forming said second semiconductor layer.

75. A process for manufacturing a semiconductor wafer as defined in claim 74, comprising the additional step of forming a protection layer on the walls of the pores in said porous layer serving as said separation layer prior to the formation of said second semiconductor layer.

76. A process for manufacturing a semiconductor wafer as defined in claim 74, comprising the additional step of conducting heat-treatment on said porous layer serving as said separation layer under a reducing atmosphere containing hydrogen prior to the formation of said semiconductor layer.

77. A process for manufacturing a semiconductor wafer as defined in claim 74, comprising the step of forming said second semiconductor layer by supplying a small amount of raw material gas which consists of said second semiconductor layer at a growth rate of 20 nm/min. or lower.

78. A process for manufacturing a semiconductor wafer as defined in claim 74, comprising the additional step of sealing the surface of said porous layer followed by conducting heat-treatment at a temperature higher than that for said sealing step prior to the formation of said second semiconductor layer, said sealing step comprising the steps of conducting heat-treatment on said porous layer under a hydrogen reducing atmosphere and/or supplying a small amount of raw material gas for said second semiconductor layer.

79. A process for manufacturing a semiconductor wafer as defined in claim 8, wherein said first member is obtained by forming a third semiconductor layer onto said second semiconductor layer made porous.

80. A process for manufacturing a semiconductor wafer as defined in claim 79, comprising the additional step of forming a protection layer on the walls of the pores in the porous layer of said second semiconductor layer made porous prior to the formation of said third semiconductor layer.

81. A process for manufacturing a semiconductor wafer as defined in claim 79, comprising the additional step of conducting heat-treatment on the porous layer of said second semiconductor layer made porous under a reducing atmosphere containing hydrogen prior to the formation of said third semiconductor layer.

82. A process for manufacturing a semiconductor wafer as defined in claim 79, comprising the step of forming said third semiconductor layer by supplying a small amount of raw material gas which consists of said third semiconductor layer at a growth rate of 20 nm/min. or lower.

83. A process for manufacturing a semiconductor wafer as defined in claim 79, comprising the additional step of sealing the surface of the porous layer of said second semiconductor layer made porous followed by conducting heat-treatment at a temperature higher than that for said sealing step prior to the formation of said third semiconductor layer, said sealing step comprising the steps of conducting heat-treatment of said porous layer under a hydrogen reducing atmosphere and/or supplying a small amount of raw material gas for said third semiconductor layer.

84. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 6, wherein the surface of said high concentration p-type silicon layer is smoothed prior to the epitaxial growth of said high concentration p-type silicon layer.

85. A process for manufacturing a semiconductor wafer as defined in claim 7 or 8, wherein said second semiconductor wafer is formed by smoothing the surface of said first semiconductor layer on said separated p-type semiconductor substrate.

86. A process for manufacturing a semiconductor wafer as defined in claim 85, wherein said smoothing step is carried out by conducting at least one treatment selected from the group consisting of surface-polishing, planing, etching, and heat-treatment.

87. A process for manufacturing a semiconductor wafer as defined in claim 86, wherein said heat-treatment is heat-treatment under a reducing atmosphere containing hydrogen.

88. A process for manufacturing a semiconductor wafer as defined in claim 87, wherein a temperature for said heat-treatment under a reducing atmosphere containing hydrogen is not lower than 800°C and not higher than the melting temperature of the component materials of said p-type semiconductor substrate.

89. A process for manufacturing a semiconductor wafer as defined in claim 7, comprising the additional step of transferring said second semiconductor layer to said second semiconductor substrate followed by removing said separation layer remaining on said second semiconductor layer.

90. A process for manufacturing a semiconductor wafer as defined in claim 8, comprising the additional step of transferring said third semiconductor layer to said second semiconductor substrate followed by removing said separation layer remaining on said second semiconductor layer.

91. A process for manufacturing a semiconductor wafer as defined in claim 89 or 90, wherein heat-treatment under a reducing atmosphere containing hydrogen is conducted after removing said remaining separation layer.

92. A process for manufacturing a semiconductor wafer as defined in any one of claims 2, 4, 5, 6, and 7, wherein said separation through said separation layer is separation caused at a part selected from the group consisting of the inside, the upper surface, and the lower surface of said separation layer.

93. A process for manufacturing a semiconductor wafer as defined in claim 8, wherein said step of transferring said third semiconductor layer onto said second member is carried out by conducting separation at a part selected from the group consisting of the inside, the upper surface, and the lower surface of said first semiconductor layer made porous.

94. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 6, wherein said semiconductor layer and said low concentration p-type silicon layer are formed by the same CVD apparatus.

95. A process for manufacturing a semiconductor wafer as defined in any one of claims 3 to 8, wherein said second semiconductor wafer is used for use other than that for said first and second members.

96. A process for manufacturing a semiconductor wafer as defined in claim 6, wherein an oxide film having a thickness of 10 nm to 10 μm is formed on the back side of said p-type silicon substrate by said heat-treatment under an oxidizing atmosphere.

97. A method for using a semiconductor wafer, characterized by preparing a seed-wafer which has been used for manufacturing a bonded SOI substrate followed by conducting smoothing treatment on at least one surface of said seed-wafer so as to be sold as a semiconductor wafer.

98. A method for using a semiconductor wafer as defined in claim 97, wherein the process for manufacturing said bonded SOI wafer comprises the steps of bonding a first member which has a monocrystalline semiconductor layer on a region of monocrystalline silicon through an insulating layer with a second member, and conducting separation through the inside and/or the surface of said separation layer.

99. A method for using a semiconductor wafer as defined in claim 98, wherein said bonding step is the step of conducting separation through an insulating layer which is formed on said monocrystalline semiconductor layer and/or said second member.

100. A method for using a semiconductor wafer as defined in claim 98, wherein said separation layer is selected from the group consisting of a porous layer which is formed by anodization treatment of a silicon substrate and a microbubble layer formed by ion implantation of at least one element selected from the group consisting of hydrogen, nitrogen, and rare gas.

101. A method for using a semiconductor wafer as defined in claim 97, wherein said smoothing treatment comprises the step of mirror finish polishing.

102. A method for using a semiconductor wafer as defined in claim 97, wherein said smoothing treatment is conducted on both sides of said seed-wafer.

103. A method for using a semiconductor wafer as defined in claim 97, wherein mirror finish polishing is conducted on both sides of said seed-wafer to be sold as said semiconductor wafer.

104. A method for using a semiconductor wafer as defined in claim 97, wherein said smoothing treatment comprises the step containing hydrogen annealing.

105. A method for using a semiconductor wafer as defined in claim 97, comprising the additional step of forming an epitaxial semiconductor layer on said seed-wafer.

106. A process for manufacturing a semiconductor wafer as defined in claim 11, wherein said separation layer and said layer made porous is each formed by anodization treatment.

FIG. 1

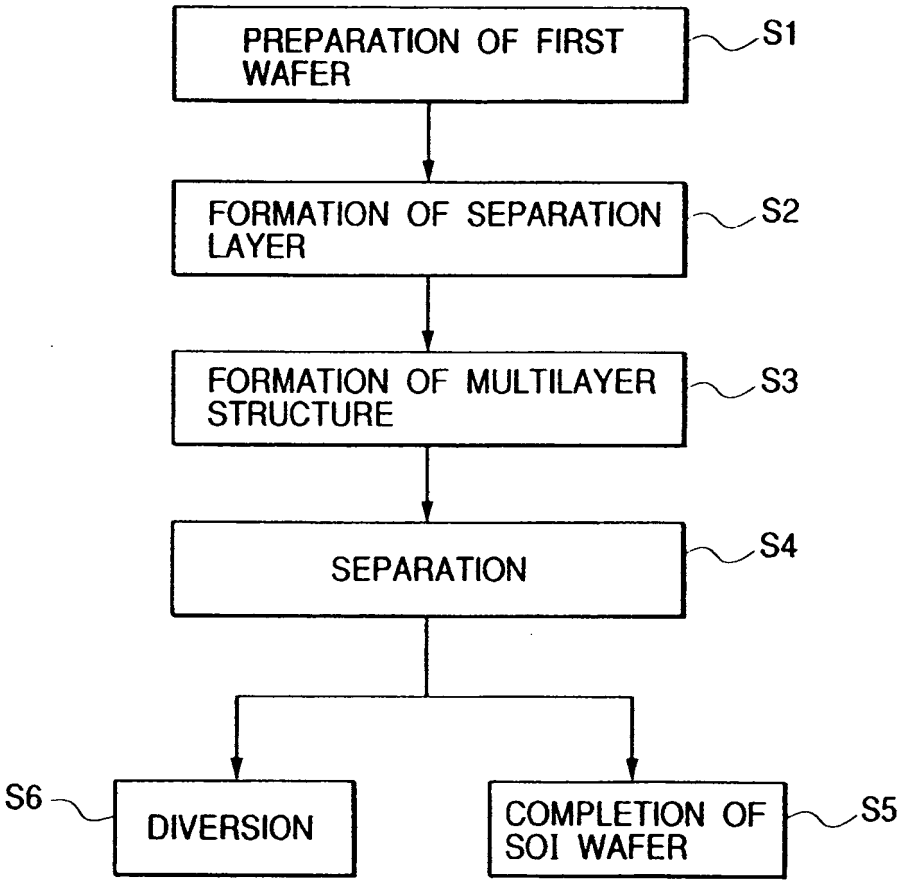


FIG. 2

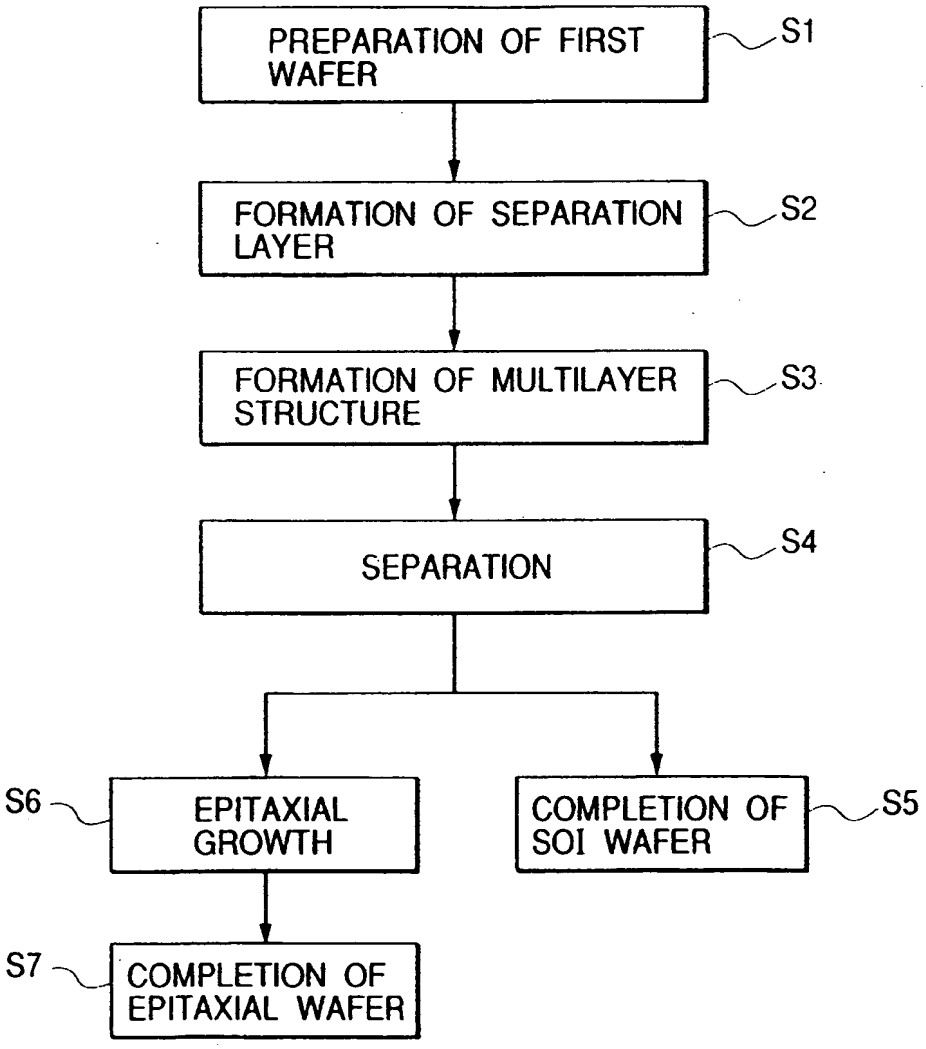


FIG. 3

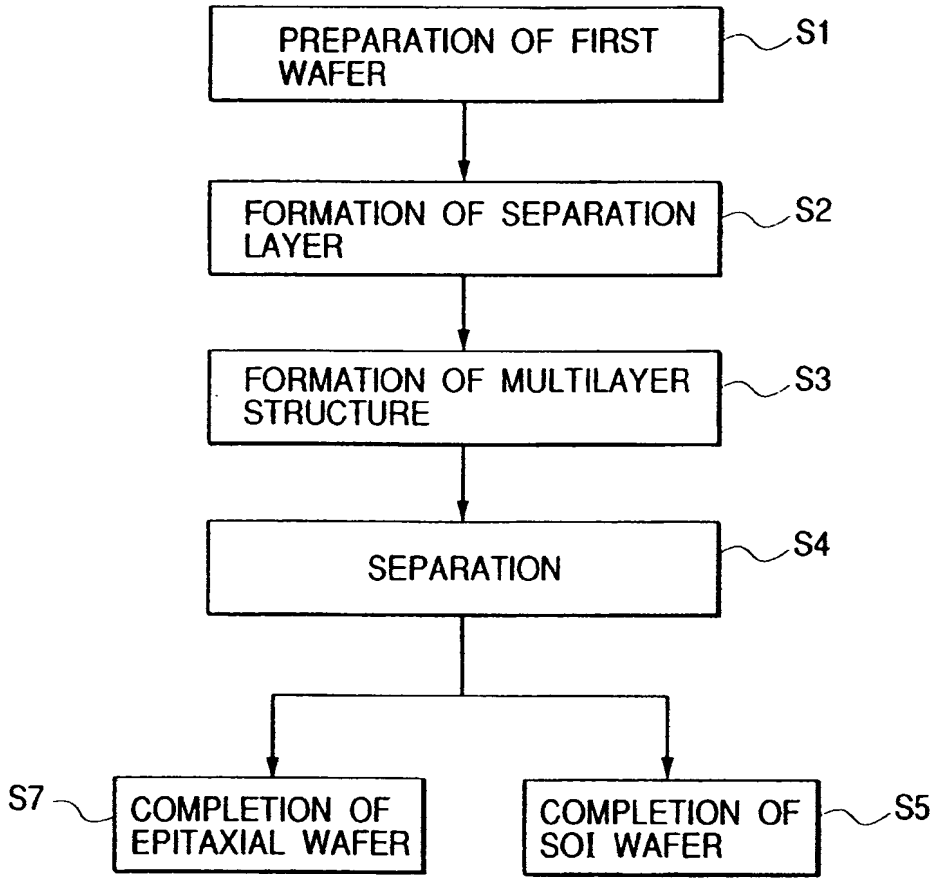


FIG. 4A

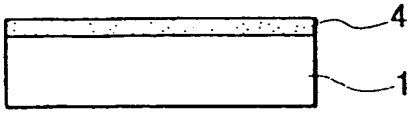


FIG. 4B

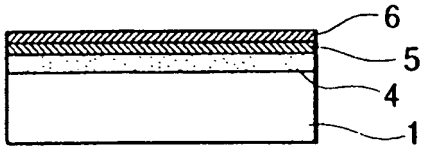


FIG. 4C

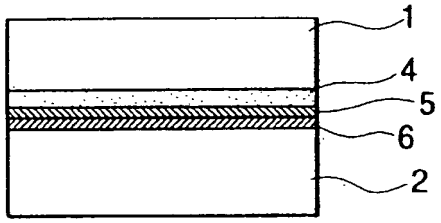


FIG. 4D

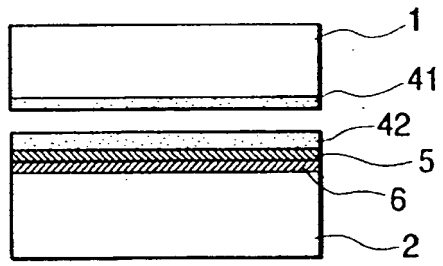


FIG. 4E

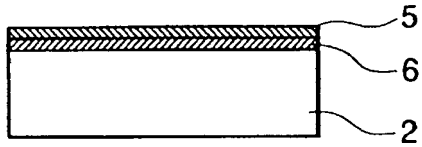


FIG. 4F

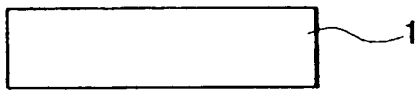


FIG. 4G

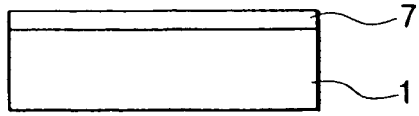


FIG. 5A

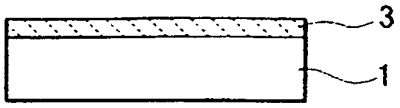


FIG. 5B

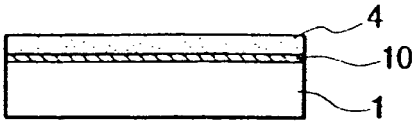


FIG. 5C

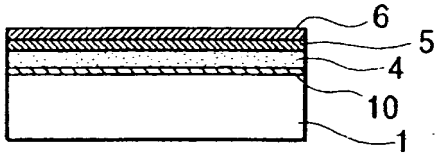


FIG. 5D

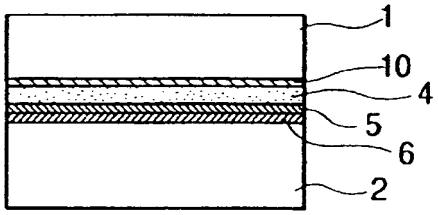


FIG. 5E

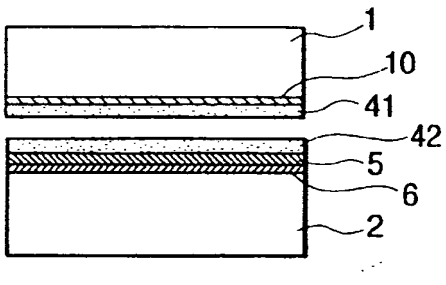


FIG. 5F

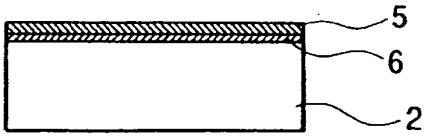


FIG. 5G

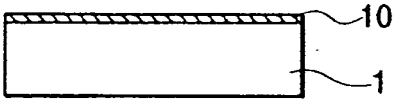


FIG. 5H

FIG. 5I

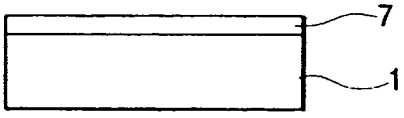


FIG. 6A

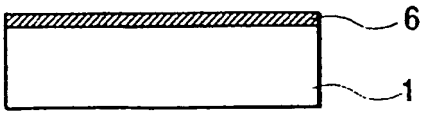


FIG. 6B

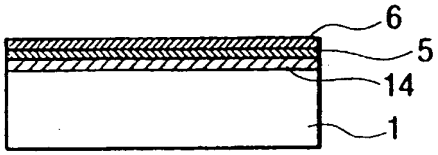


FIG. 6C

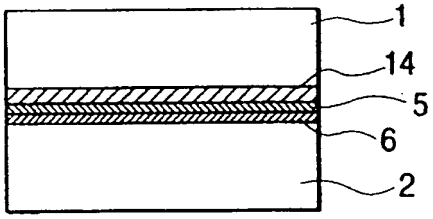


FIG. 6D

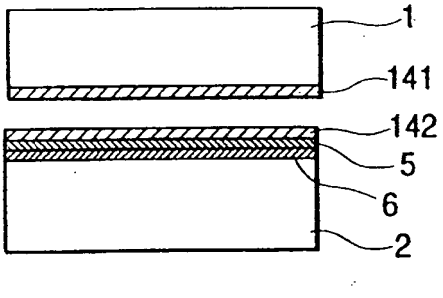


FIG. 6E

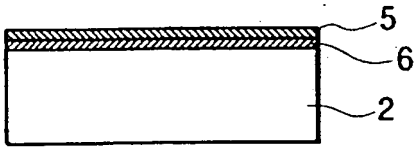


FIG. 6F

FIG. 6G

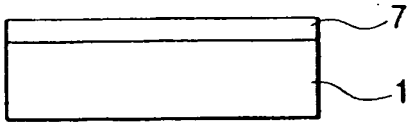


FIG. 7A

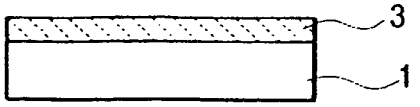


FIG. 7B

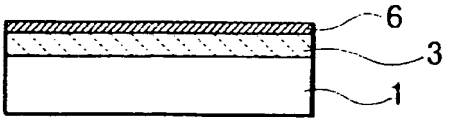


FIG. 7C

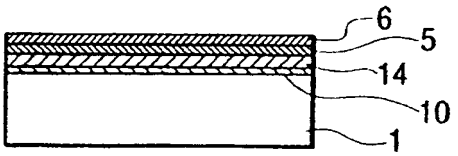


FIG. 7D

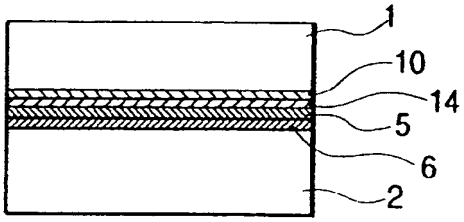


FIG. 7E

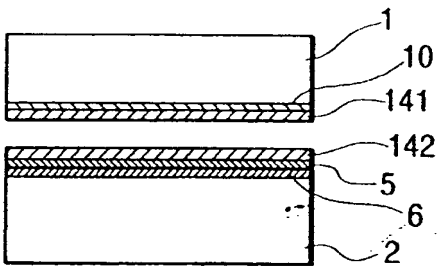


FIG. 7F

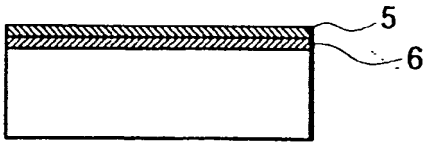


FIG. 7G

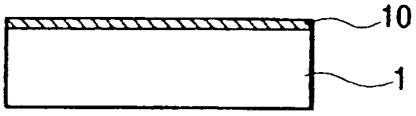


FIG. 7H

FIG. 7I

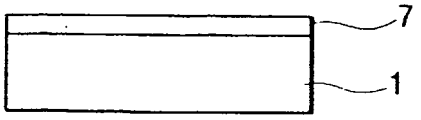


FIG. 8A

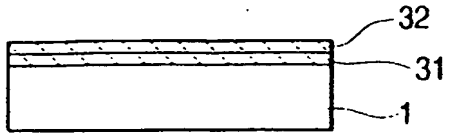


FIG. 8B

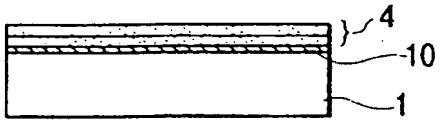


FIG. 8C

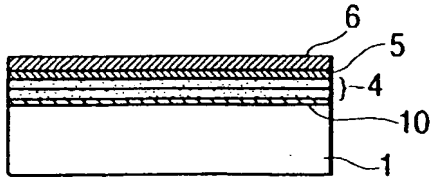


FIG. 8D

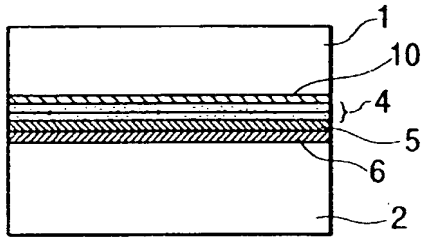


FIG. 8E

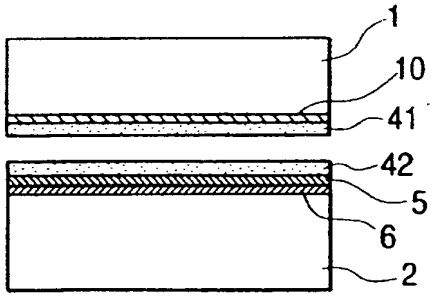


FIG. 8F

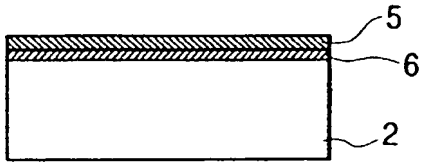


FIG. 8G

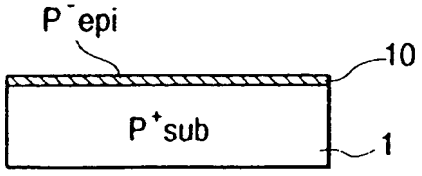


FIG. 9A

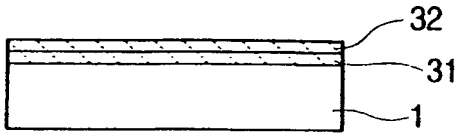


FIG. 9B

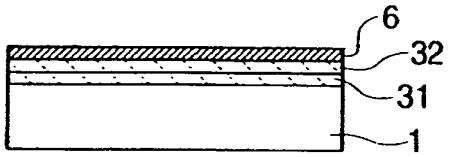


FIG. 9C

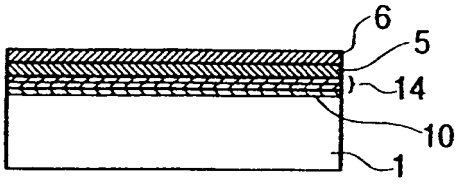


FIG. 9D

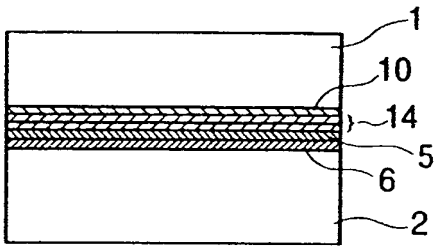


FIG. 9E

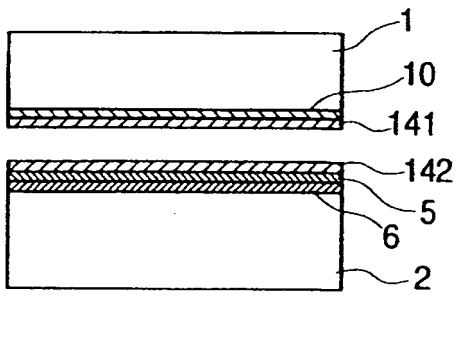


FIG. 9F

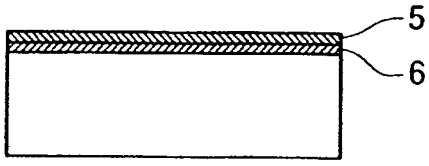


FIG. 9G

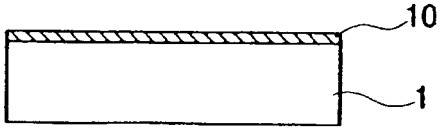


FIG. 10

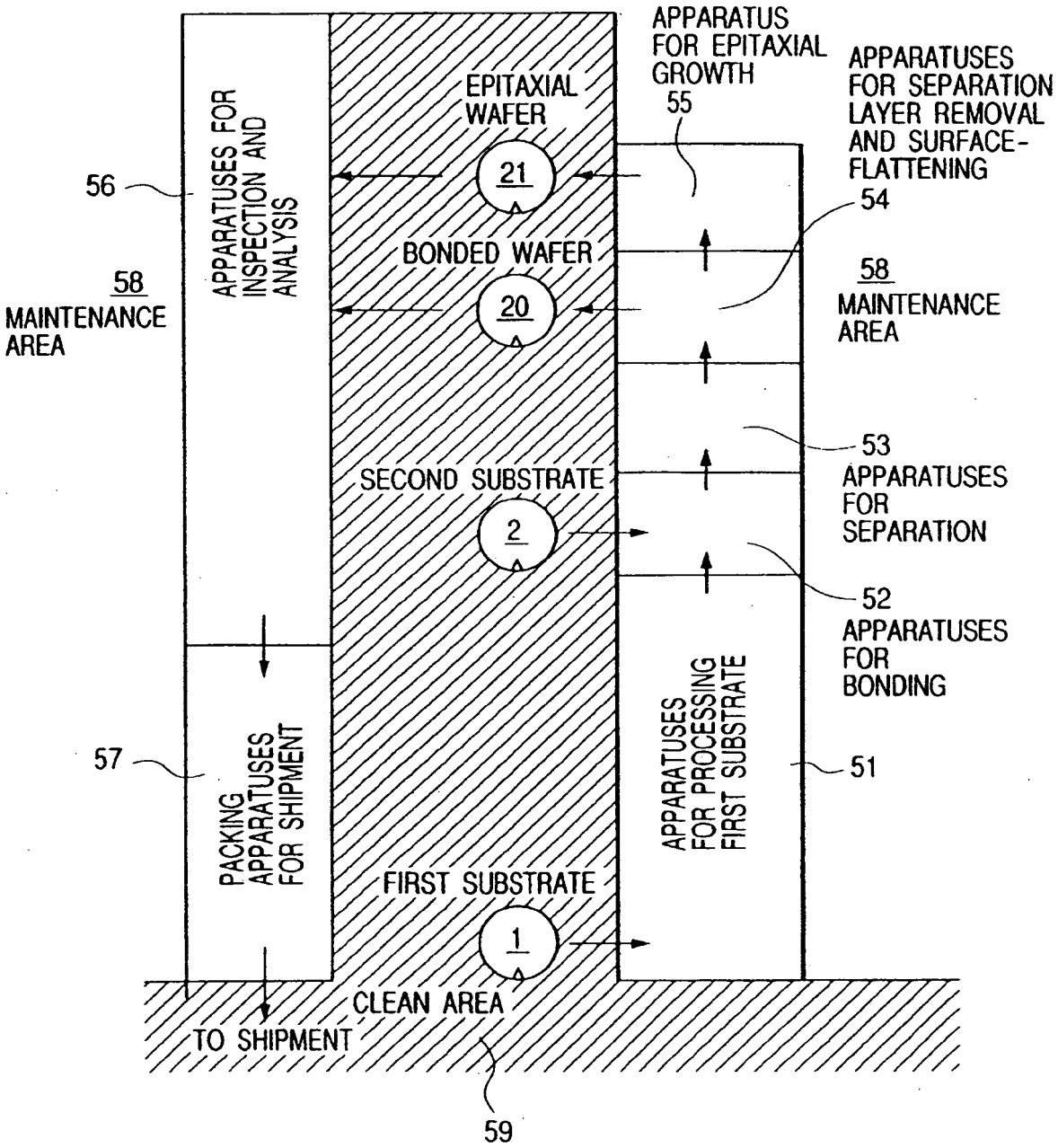


FIG. 11

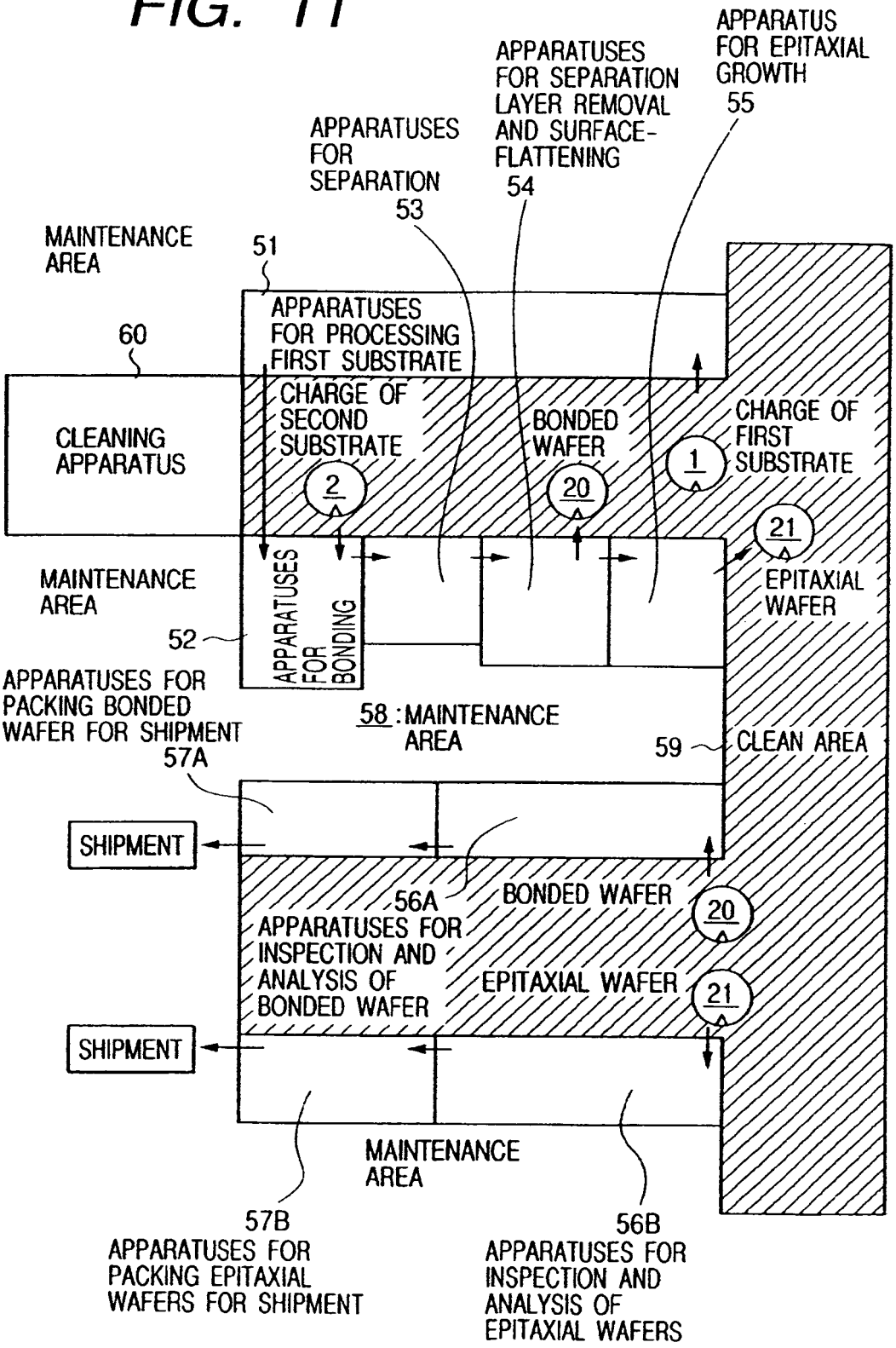


FIG. 12

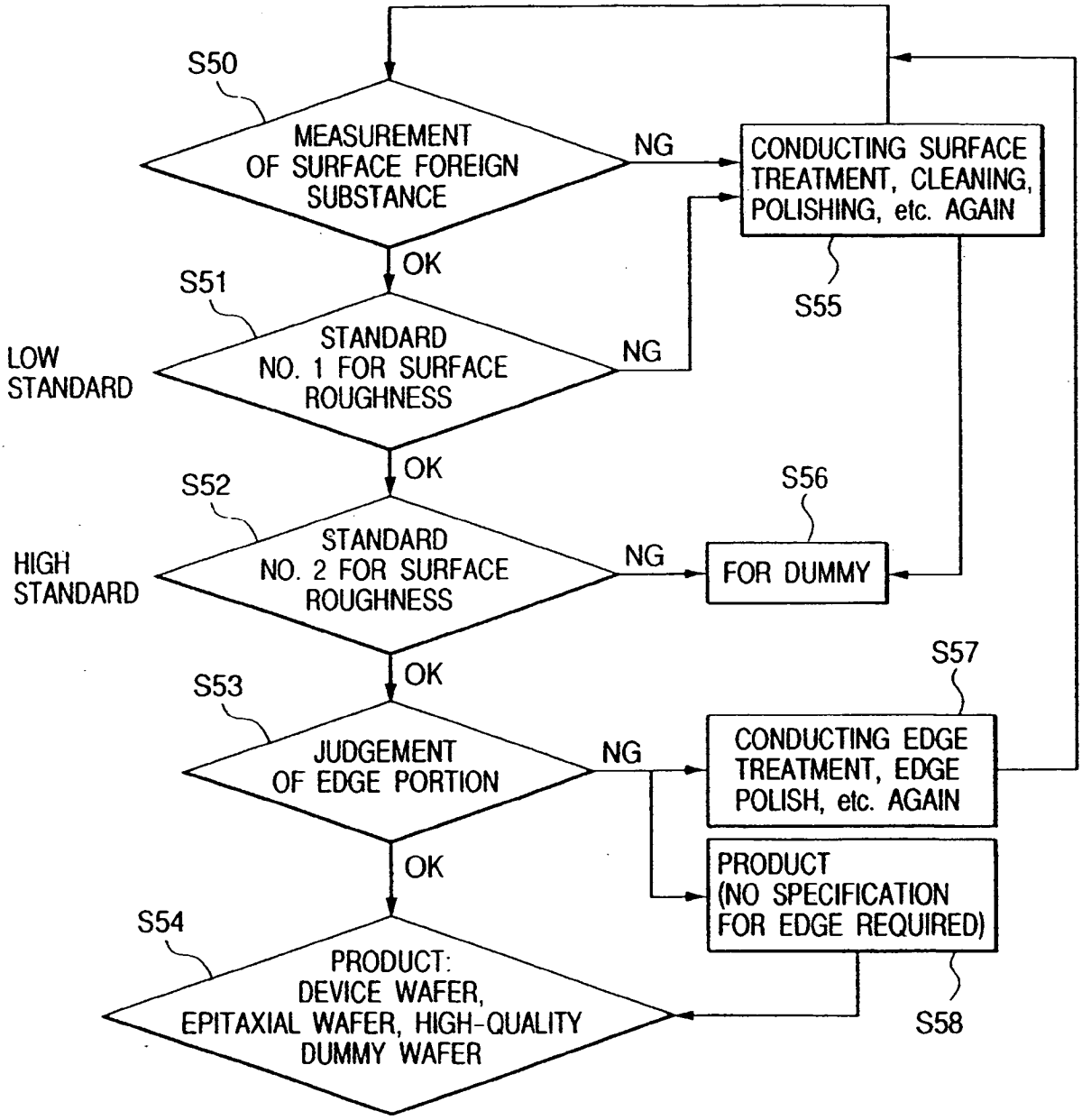


FIG. 13

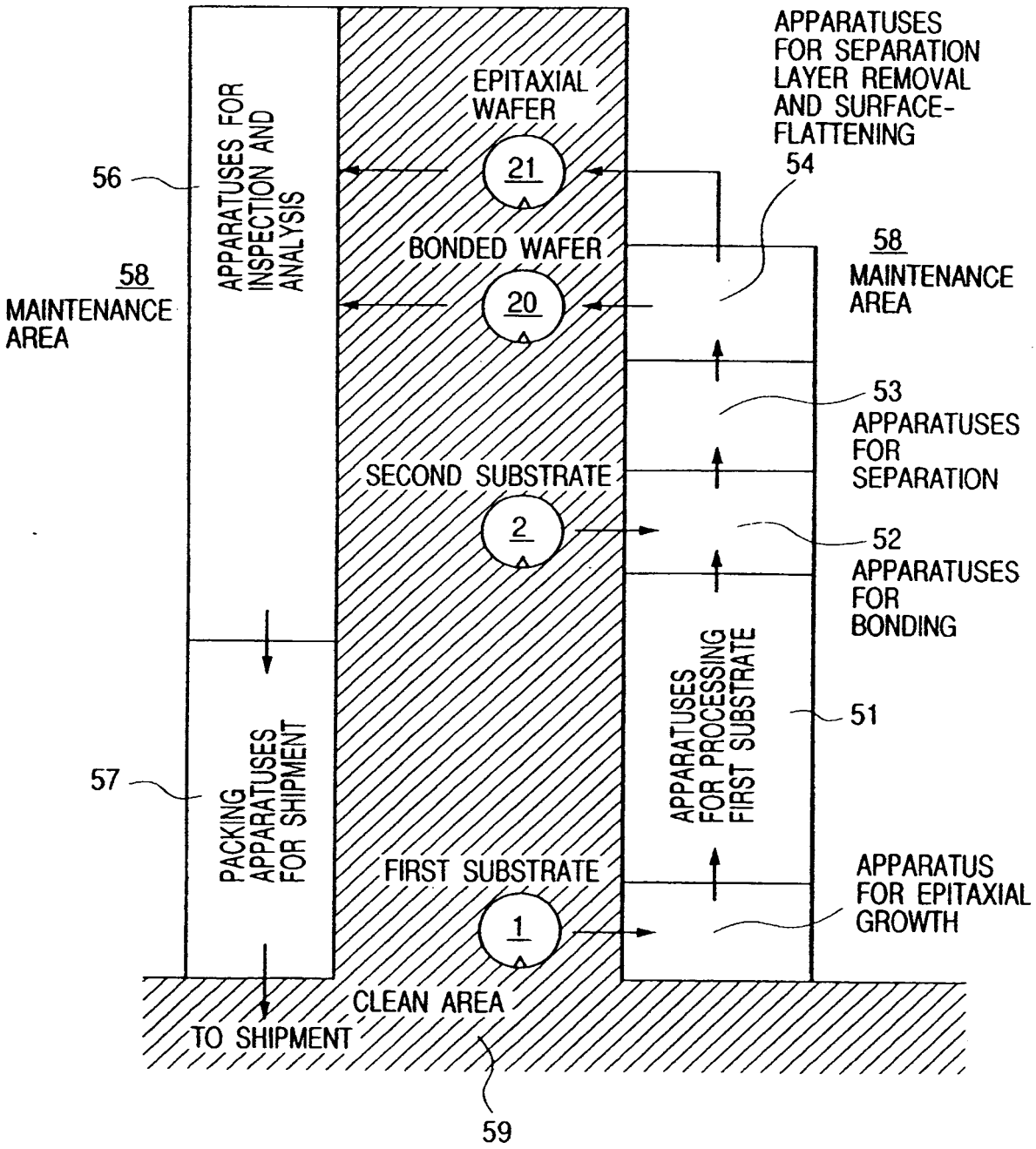


FIG. 14

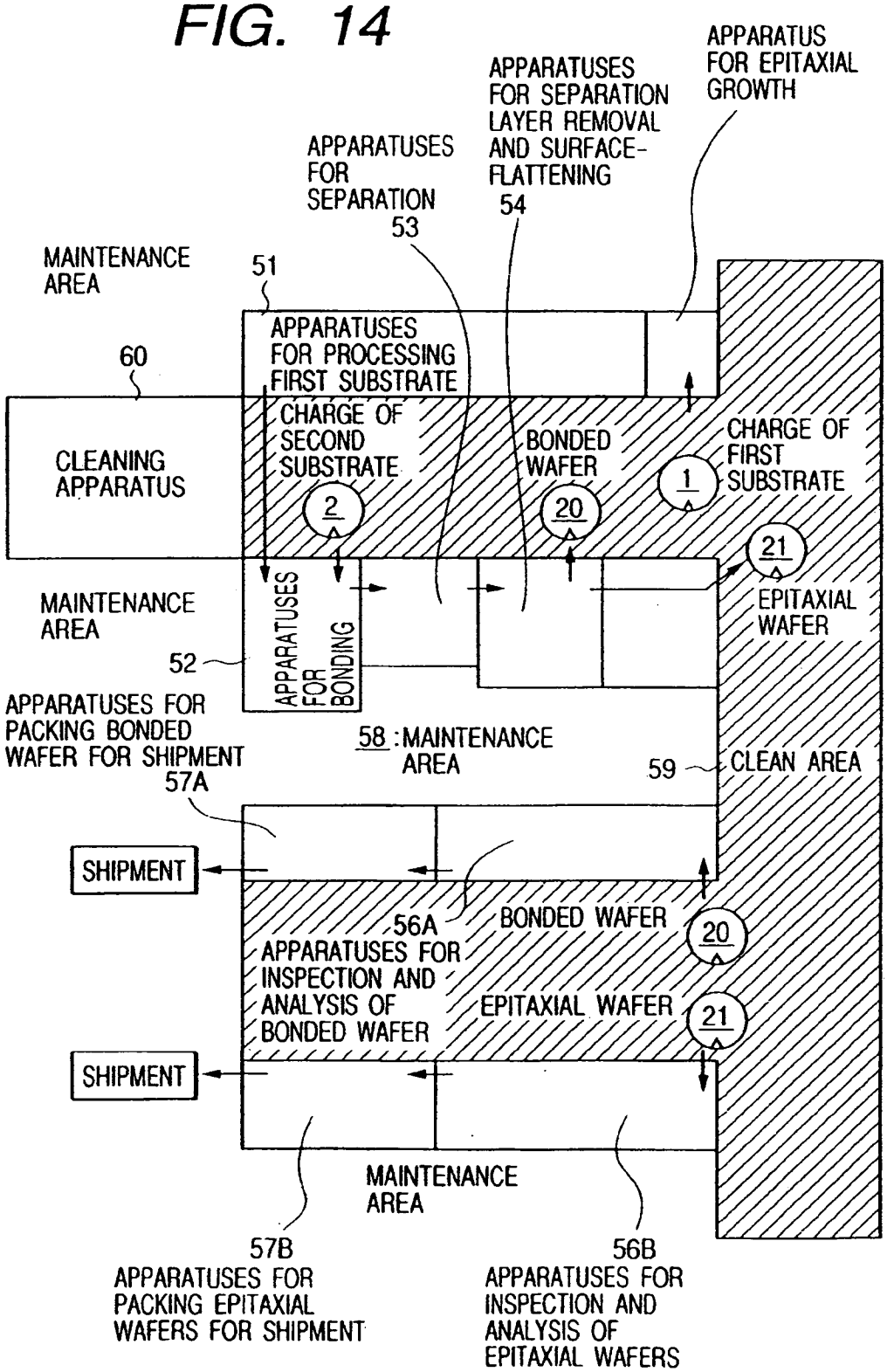


FIG. 15A

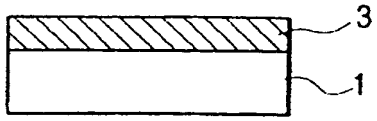


FIG. 15B

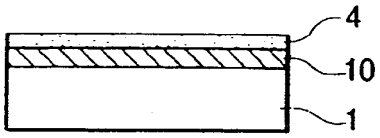


FIG. 15C

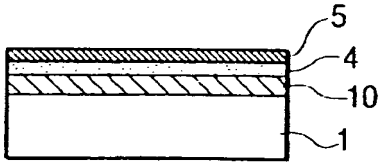


FIG. 15D

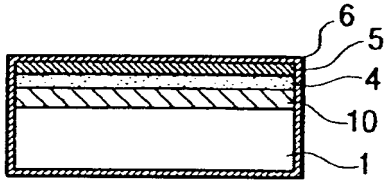


FIG. 15E

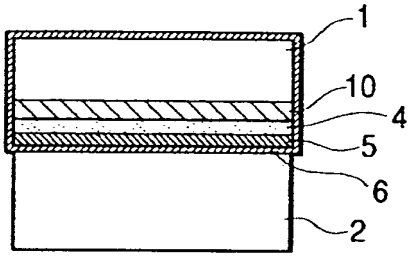


FIG. 15F

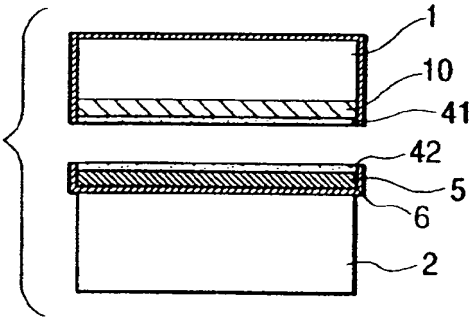


FIG. 15G

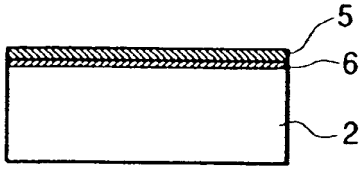


FIG. 15H

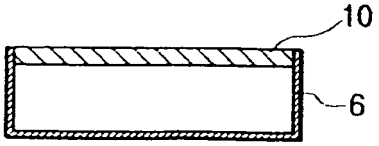


FIG. 16A

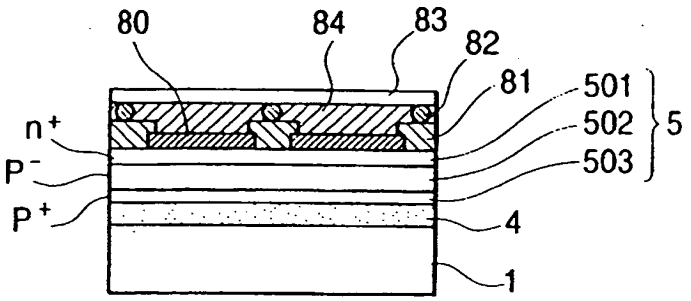


FIG. 16B

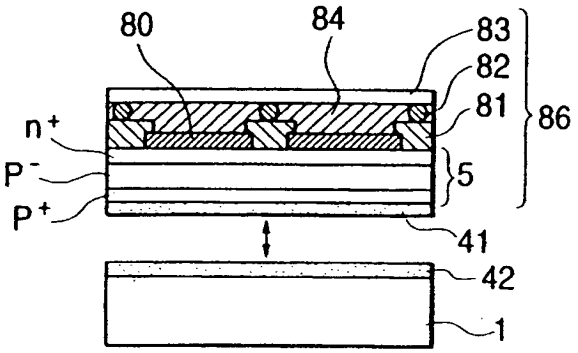


FIG. 16C

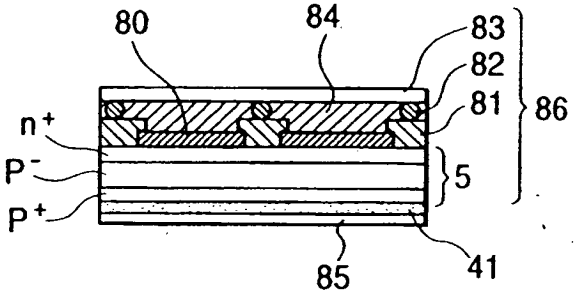


FIG. 16D

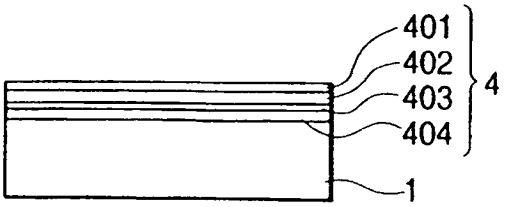


FIG. 17A

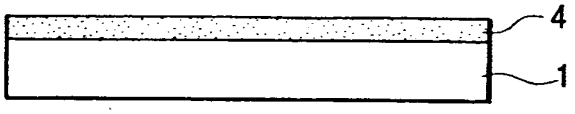


FIG. 17B

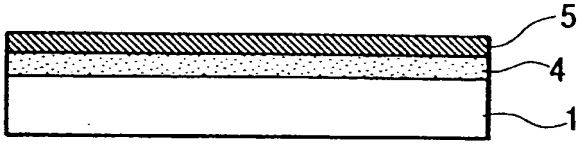


FIG. 17C

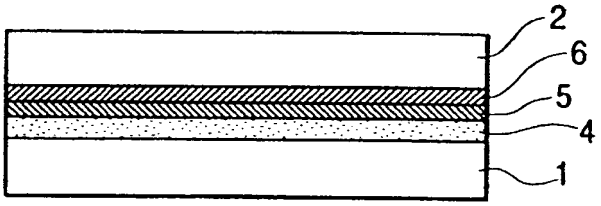


FIG. 17D

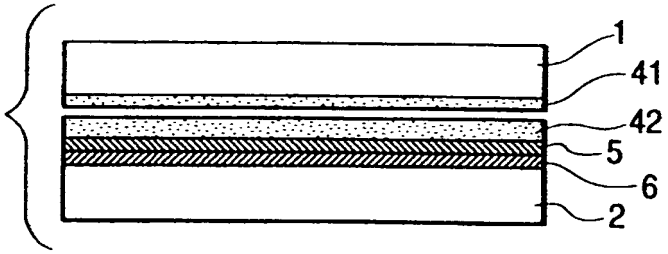
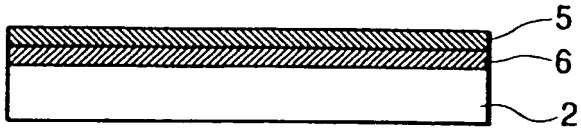


FIG. 17E



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(54) Method of manufacturing semiconductor wafer method of using and utilizing the same

(57) A process for manufacturing a semiconductor wafer which has superior suitability for mass production and reproducibility. The process comprises the steps of preparing a first member which has a monocrystalline semiconductor layer on a semiconductor substrate with a separation layer arranged therebetween with a semiconductor wafer as the raw material, transferring the monocrystalline semiconductor layer onto a second member which comprises a semiconductor wafer after separating the monocrystalline semiconductor layer through the separation layer, and smoothing the surface of the semiconductor substrate after the transferring step so as to be used as a semiconductor wafer for purposes other than forming the first and second members.

FIG. 4A

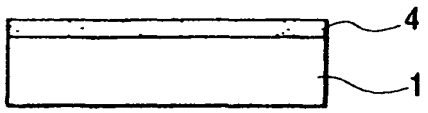

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FIG. 4B

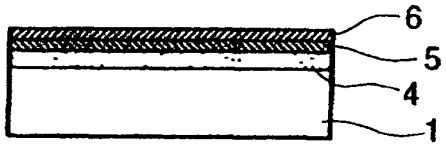


FIG. 4C

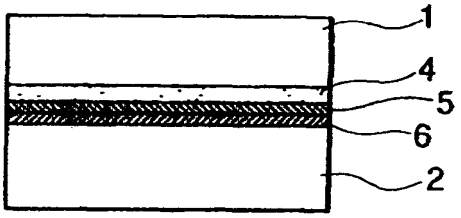


FIG. 4D

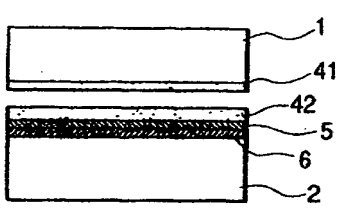


FIG. 4E

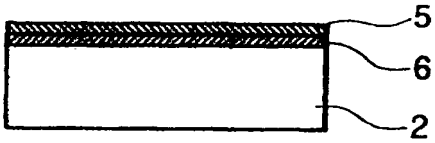
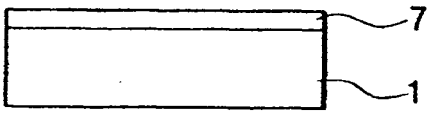


FIG. 4F

FIG. 4G



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9737

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	EP 0 843 346 A (CANON KK) 20 May 1998 (1998-05-20) * abstract; claims; figures * * page 7, line 50 - line 52 *	1-106	H01L21/20 H01L21/762
Y	US 5 131 979 A (LAWRENCE JOHN E) 21 July 1992 (1992-07-21) * abstract; claims; figures *	1-106	
A	EP 0 774 776 A (KOBE STEEL LTD ;KOBE PRECISION INC (US)) 21 May 1997 (1997-05-21) * abstract; claims; figures *	1,2,38, 39	
A	EP 0 767 486 A (CANON KK) 9 April 1997 (1997-04-09) * abstract; claims; figures * * column 12, line 55 - column 13, line 28 *	1-8,97	
A	EP 0 793 263 A (CANON KK) 3 September 1997 (1997-09-03) * abstract; claims; figures *	6	TECHNICAL FIELDS SEARCHED (Int.Cl.7) H01L
A	EP 0 553 859 A (CANON KK) 4 August 1993 (1993-08-04) * abstract; claims; figures *	2,7,8, 15,16, 74-76, 79-81	
A	EP 0 867 922 A (CANON KK) 30 September 1998 (1998-09-30) * abstract; claims; figures *	2,7,8, 15,19, 74,78, 79,83	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 August 2001	Wirner, C

CATEGORY OF CITED DOCUMENTS

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EUROPEAN SEARCH REPORT

Application Number
EP 99 30 9737

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	WO 98 52216 A (HENLEY FRANCOIS J ;CHEUNG NATHAN W (US); SILICON GENESIS CORP (US)) 19 November 1998 (1998-11-19) * abstract; claims; figures *	1-3,26, 32,53, 59,60	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	31 August 2001	Wirner, C

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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31-08-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0843346 A	20-05-1998	AU 4517497 A	21-05-1998
		CN 1191383 A	26-08-1998
		JP 10200079 A	31-07-1998
		SG 54593 A	16-11-1998
		US 6054363 A	25-04-2000
US 5131979 A	21-07-1992	NONE	
EP 0774776 A	21-05-1997	US 5855735 A	05-01-1999
		JP 9171981 A	30-06-1997
		KR 236991 B	15-01-2000
EP 0767486 A	09-04-1997	JP 9162090 A	20-06-1997
		CA 2187269 A	07-04-1997
		CN 1159071 A	10-09-1997
		SG 63669 A	30-03-1999
		US 6246068 B	12-06-2001
		US 5854123 A	29-12-1998
EP 0793263 A	03-09-1997	JP 9237884 A	09-09-1997
		CA 2198552 A	28-08-1997
		CN 1169025 A	31-12-1997
		KR 238571 B	15-01-2000
		SG 55280 A	21-12-1998
EP 0553859 A	04-08-1993	JP 5217827 A	27-08-1993
EP 0867922 A	30-09-1998	AU 728331 B	04-01-2001
		AU 5969998 A	01-10-1998
		CA 2233115 A	27-09-1998
		CN 1199920 A	25-11-1998
		JP 10326882 A	08-12-1998
		KR 260832 B	01-07-2000
		SG 68658 A	16-11-1999
		TW 404061 B	01-09-2000
		US 6143628 A	07-11-2000
WO 9852216 A	19-11-1998	US 5994207 A	30-11-1999
		US 6155909 A	05-12-2000
		AU 7685198 A	08-12-1998
		CN 1255237 T	31-05-2000
		EP 0995227 A	26-04-2000
		US 6013567 A	11-01-2000
		US 6033974 A	07-03-2000
		US 6048411 A	11-04-2000
		US 6159824 A	12-12-2000

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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 99 30 9737

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31-08-2001

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9852216 A		US 5985742 A	16-11-1999
		US 6146979 A	14-11-2000
		US 6013563 A	11-01-2000
		US 6010579 A	04-01-2000
		US 6159825 A	12-12-2000
		US 6245161 B	12-06-2001
		US 6162705 A	19-12-2000
		US 6187110 B	13-02-2001

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